

## **40Gbps QSFP+ LR4 PSM**

### **QSFP-LR4-PSM**

#### **Features**

- Four-channel full-duplex transceiver modules
- Transmission data rate up to 10.7Gbit/s per channel
- Up to 10km transmission of single mode fiber
- Low power consumption <3.5W
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- Hot Pluggable QSFP form factor
- Single MPO connector receptacle
- Built-in digital diagnostic function
- RoHS-6 compliant

#### **Applications**

- InfiniBand QDR, DDR and SDR
- 40G Ethernet
- Proprietary High Speed Interconnections
- Datacenter and Enterprise Networking

#### **Product Description**

This product is a parallel 40Gb/s Quad Small Form-factor Pluggable (QSFP+) optical module. It provides increased port density and total system cost savings. The QSFP+ full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10Gb/s operation for an aggregate data rate of 40Gb/s on 10km of single mode fiber.

An optical fiber ribbon cable with an MTP/MPO connector can be plugged into the QSFP+ module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a z-pluggable 38-pin connector per MSA requirement.

The module operates with single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module can be managed through the I2C two-wire serial interface.

This product is a QSFP+ parallel single mode optical transceiver with an MTP/MPO fiber ribbon connector. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 10.3Gb/s per channel. Figure 1 shows the functional block diagram of this product.

## Transceiver Block Diagram

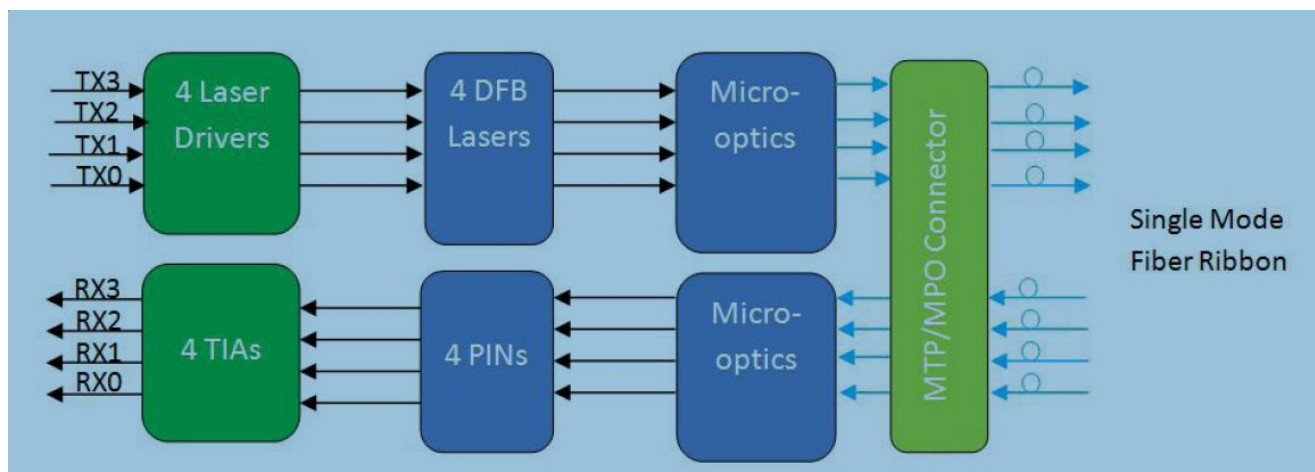


Figure 1. Transceiver Block Diagram

### Absolute Maximum Rating

The operation in excess of any absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Ts	-40	85	°C	1
Operating Case Temperature	Top	0	70	°C	
3.3V Power Supply Voltage	Vcc	-0.3	3.6	V	
Data Input Voltage- Single Ended	Vin	-0.3		Vcc+0.3	
Control Input Voltage	V	-0.3	3.6	V	
Relative Humidity	RH	0	85	%	2
Damage Threshold, each lane	THd	3.3		dBm	

Notes:

1. Limited by the fiber cable jacket, not the active ends.
2. Non-condensing.

### Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Note
Case Operating Temperature	Top	0		70	°C	
Power Supply Voltage	Vcc	3.13	3.3	3.47	V	
Date Rate per Channel	DR		10.3	10.7	Gbps	
Bit Error Ratio (BER)	BER		10-12			1, 2
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate				400	kHz	
Differential Data Input / Output Load			100		Ohms	+/- 10%
Link Distance with G.652	D	0.002		100	km	

Notes:

1. Bit-Error-Rate (BER) is tested with PRBS 2<sup>31</sup>-1 pattern.
2. 40G QSFP AOC cable requires an electrical connector compliant with SFF-8643 which is used on the host board in order to guarantee its electrical interface specification.

**Electrical Characteristics**

All parameters are specified under the recommended operating conditions with PRBS31 data pattern unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Unit	Note
<b>Transceiver Electrical Characteristics</b>						
TRx Power Consumption				3.5	W	
TRx Supply Current				1.1	A	
TRx Power-on Initialization Time				2000	ms	1
Input Logic Level High	V <sub>IH</sub>	2.0		VCC	V	
Input Logic Level Low	V <sub>IL</sub>	0		0.8	V	
Output Logic Level High	V <sub>OH</sub>	VCC-0.5		VCC	V	
Output Logic Level Low	V <sub>OL</sub>	0		0.4	V	
<b>Transmitter (each Lane)</b>						
Single Ended Input Voltage (Referred to TP1 signal common)		-0.4		3.3	V	2
AC Common-Mode Input Voltage (RMS)				15	mV	RMS
Differential input voltage Swing Threshold	V <sub>in,pp</sub>	50			mV	LOSA Threshold
Differential input voltage amplitude	ΔV <sub>in</sub>	300		1100	mVp-p	
Differential input impedance	Z <sub>in</sub>	90	100	110	ohm	
Differential Input Return Loss	S <sub>dd11</sub>	See IEEE 802.3ba 86A.4.11			dB	10MHz-11.1GHz
J2 Jitter Tolerance	J <sub>t2</sub>	0.17			UI	
J9 Jitter Tolerance	J <sub>t9</sub>	0.29			UI	
Data Dependent Pulse Width Shrinkage (DDPWS ) Tolerance		0.07			UI	
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.11, 0.31 95, 350			UI	Hit Ratio = 5x10 <sup>-5</sup>
<b>Receiver (each Lane)</b>						
Single Ended Output Voltage(Referred to signal common)		-0.3		4	V	
AC Common-Mode Output Voltage (RMS)				7.5	mV	RMS
Differential Output voltage Swing Threshold	V <sub>out,pp</sub>	50			mV	
Differential Output voltage amplitude	ΔV <sub>Out</sub>	500		800	mVp-p	
Differential Output impedance	Z <sub>Out</sub>	90	100	110	ohm	
Termination Mismatch at1MHz				5	%	

Differential Output Return Loss	Sdd <sub>11</sub>	See IEEE 802.3ba 86A.4.2.1			dB	10MHz-11.1GHz
Common Mode Output Return Loss	SCC <sub>11</sub>	See IEEE 802.3ba 86A.4.2.2			dB	10MHz-11.1GHz
Output Transition Time		28			ps	
J2 Jitter Output	Jo2			0.42	UI	
J9 Jitter Output	Jo9			0.65	UI	
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.29, 0.5 150, 425			UI	Hit Ratio = 5x10 <sup>-5</sup>

**Notes:**

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

**Optical Characteristics**

All parameters are specified under the recommended operating conditions with PRBS31 data pattern unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Unit	Note
<b>Transmitter (each Lane)</b>						
Center Wavelength	λC	1260	1310	1355	nm	1
Side Mode Suppression Ratio	SMSR	30			dB	1
Average Launch Power, each lane	PAVG	-5.5	-2.5	+1.5	dBm	
Optical Modulation Amplitude (OMA)	POMA	-4.5	-2.5	+2.5	dBm	1
Total Average Launch Power	PT			7.5	dBm	
Difference in Launch Power between any two lanes	Ptx,diff			6.5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane	OMA-TDP	-5.5	-		dBm	1
Rise/Fall Time	Tr/Tf			50	ps	
TDP, each Lane	TDP			3.2	dB	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	Rin			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			12	dB	
Transmitter Eye Mask Margin	EMM	10			%	2
Transmitter Reflectance	RT			-12	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25,				

		0.28, 0.4}				
<b>Receiver (each Lane)</b>						
Center Wavelength	$\lambda_C$	1260	1310	1355	nm	
Damage Threshold	THd	+3.3			dBm	3
Overload, each lane	OVL	2.5			dBm	
Receiver Sensitivity in OMA, each Lane	SEN	-12.5		1.5	dBm	
Receiver Reflectance	$R_R$			-12	dB	
Receive Power (OMA),each Lane				2.5	dBm	
Difference in Receive Power between any two Lanes (OMA)	Prx,diff			7.5	dB	
Signal Loss Assert Threshold	LOSA	-30			dBm	
Signal Loss Dessert Threshold	LOSD			-15	dBm	
LOS Hysteresis	LOSH	0.5		6	dB	
Optical Return Loss	ORL			-12	dBm	
Receive Electrical 3 dB upper Cutoff Frequency, each Lane	$F_c$			12.3	GHz	

**Notes:**

1. Transmitter wavelength, Side Mode Suppression Ratio and power need to meet the OMA minus TDP specs to guarantee link performance. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
2. The eye diagram is tested with 1000 waveform.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

**Digital Diagnostic Functions**

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating Temperature range
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

**Notes:**

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

### QSFP Module Pad Assignments and Descriptions

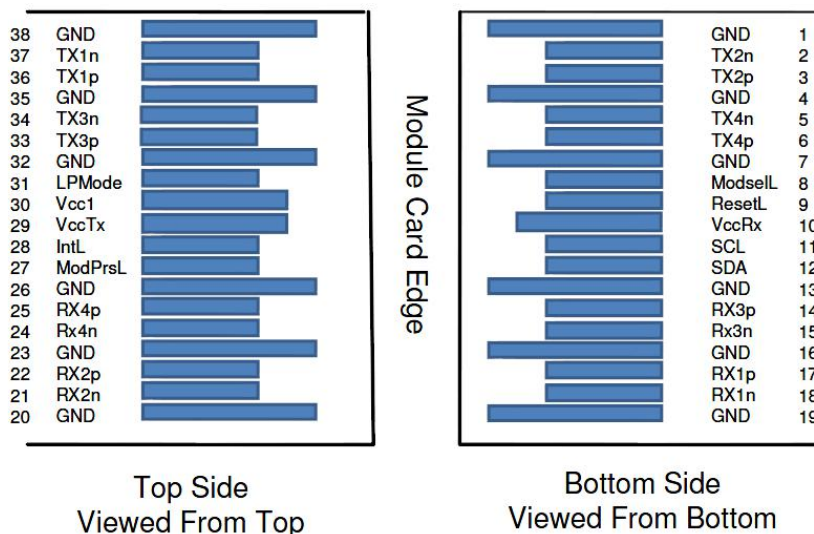


Figure 2. QSFP+ Transceiver Electrical Connector Layout

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	

23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMODE	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
<p>1: GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.</p> <p>2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table. Recommended host board power supply filtering is shown in Figures. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP Module in any combination. The connector pins are each rated for a maximum current of 500mA.</p>					

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. Per MSA the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMODE, ModPrsL and IntL.

**ModSelL** : Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus - individual ModSelL lines for each QSFP+ module must be used.

**SCL**: Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

**ResetL** : The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data\_Not\_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

**LPMODE**: Low Power Mode (LPMODE) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

**ModPrsL** : Module Present (ModPrsL) is a signal local to the host board which, in the



absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.

**IntL :** Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

### Recommended Host Board Power Supply Circuit

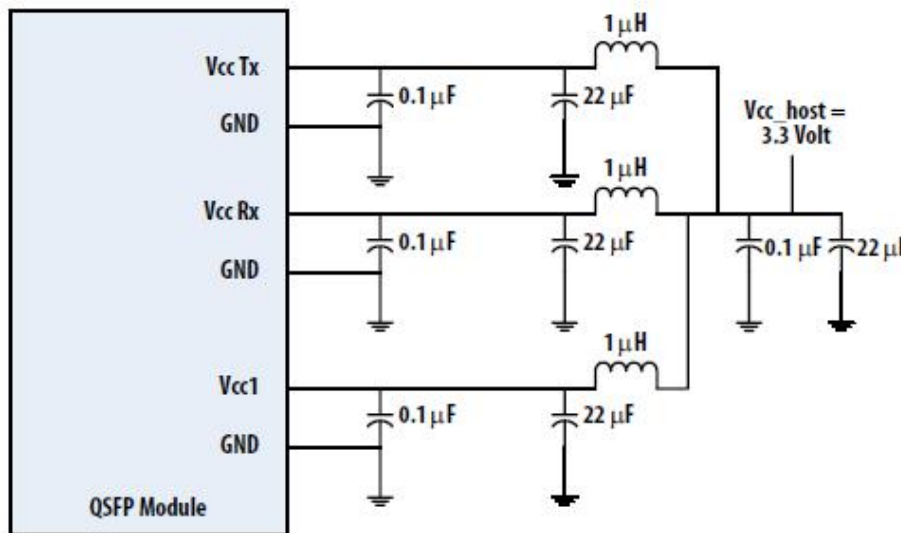


Figure 3. Recommended Power Supply Filter

### Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP SFF-8636 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.

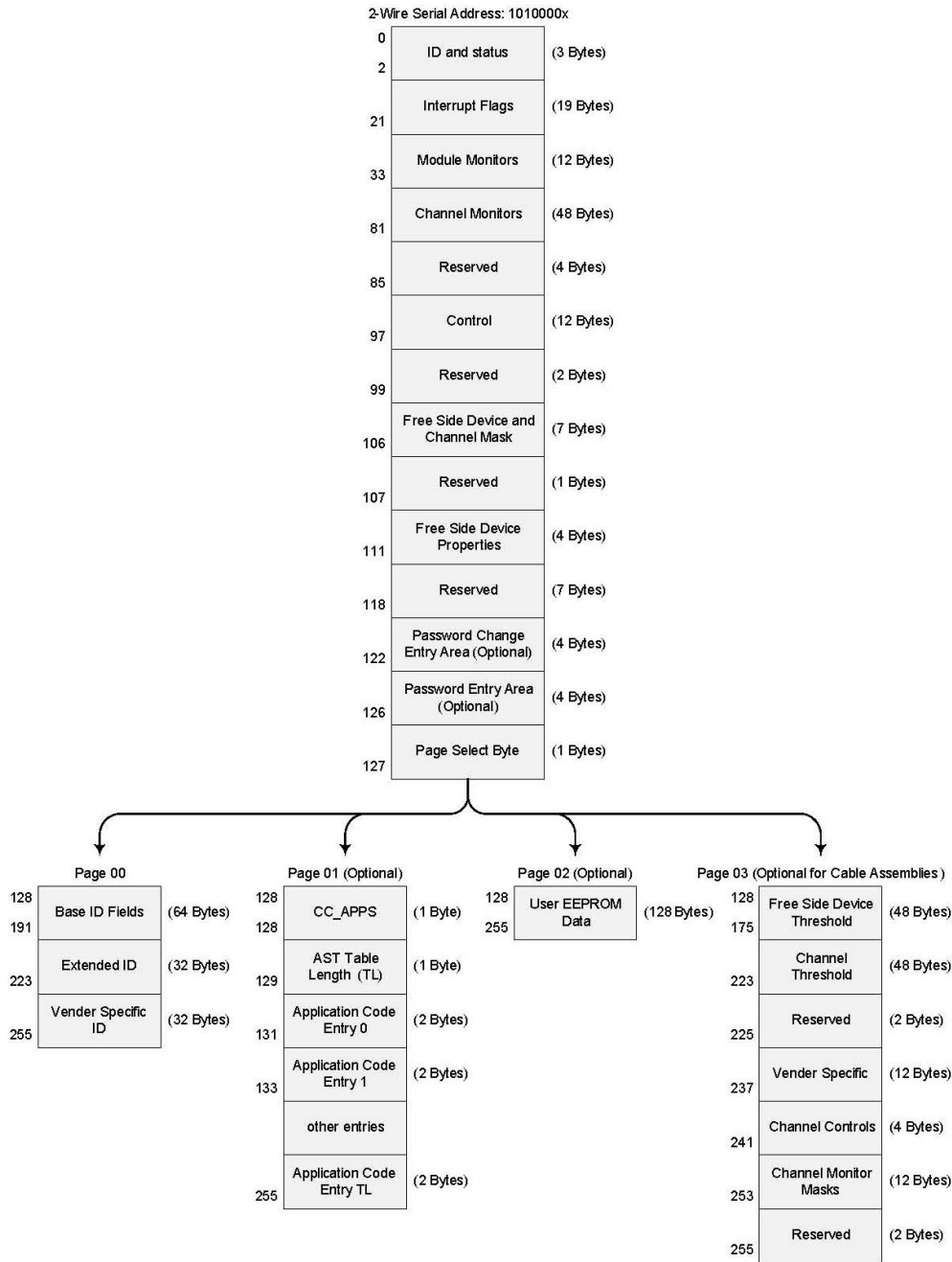


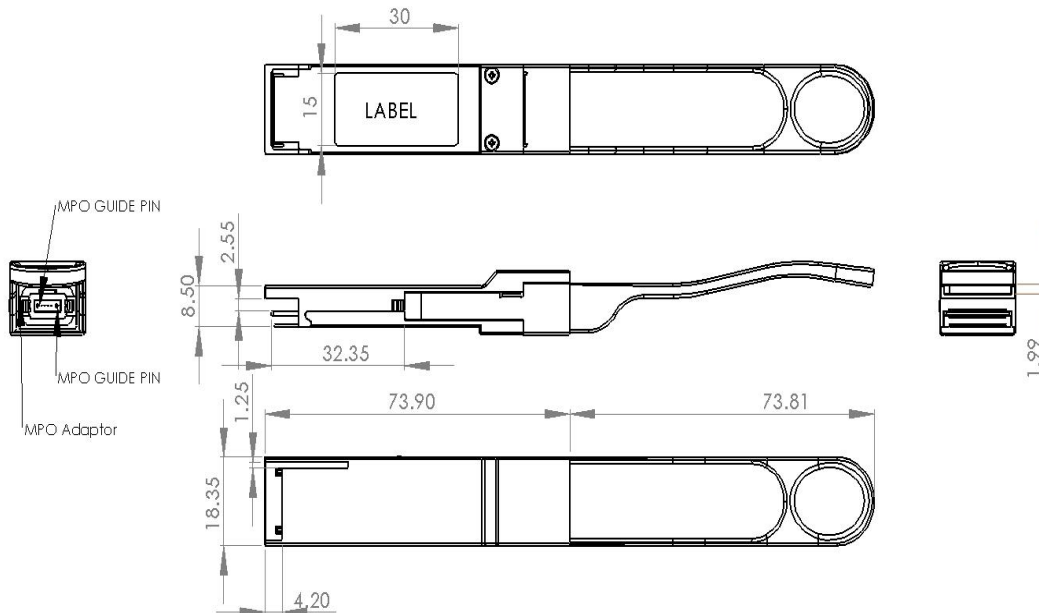
Figure4. Memory Map

Data Address (Dec)	Name of Field	Description	Value(Hex)
<b>Base ID Fields</b>			
128	Identifier	QSFP+	D
129	Extended Identifier	3.5W max. power consumption	C0
130	Connector type	MPO Fiber Connector	C

131	Transceiver Application supported	Reserved	80
132		0	
133		0	
134		Reserved	0
135		Intermediate distance	20
136		Shortwave laser w/o OFC (SN)	10
137		Single Mode (SM)	01
138		1200 Mbytes/Sec	80
139	Encoding	NRZ	03
140	BR, nominal	Nominal bit rate	67
141	Rate Select	QSFP Rate Select Version 1	0
142	Link Length(Standard SM Fiber)	10KM	A
143	Link Length(OM3)	Not supported	0
144	Link Length(OM2)	Not supported	0
145	Link Length(OM1)	Not supported	0
146	Link Length(Cooper)	Not supported	0
147	Device Tech	Un cooled transmitter device;1310nm DFB; No wavelength control; PIN detector; Transmitter not tunable	40
148~163	Vendor Name	10Gtek	
164	Electronic or optical interfaces for InfiniBand	4x SDR Speed(2.5Gb/s),DDR Speed(5.0Gb/s),QDR Speed(10Gb/s).	7
165	Vendor OUI	68	44
166		124	7C
167		127	7F
168-183	Vendor PN	QSFP-LR4-PSM	
184	Vendor Rev	REV.1A	31
185			41
186	Wavelength	1310nm	66
187			58
188	Wavelength Tolerance	±50	27
189			10
190	Max Case Temp	Max Case Temp 70°C	46
191	Check Sum	Address 128-190	

Extended ID Fields			
192	Options	Rate Select, TX Disable, TX Fault, LOS, Warning indicators for: Temperature, VCC, RX power, TX Bias	0
193			0
194			0
195			DE
196~211	Vendor SN	Serial number provided by vendor(ASCII)	
212~217	Date Code	Programmed with manufacturing date	
218	Lot Number	Programmed with manufacturing lot	
219			
220	Diagnostic Monitoring Type		8
221	Enhanced Options		0
222	Reserved	Reserved	Reserved
223	CC_EXT	Address 192-222	
Vendor Specific ID Fields			
224-255	Vendor Specific EEPROM		

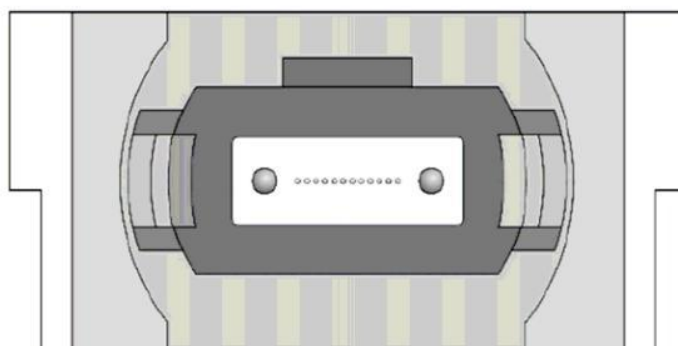
**Mechanical Design Diagram**



**Figure 5. Mechanical Outline**

### Optical Interface Lanes and Assignment

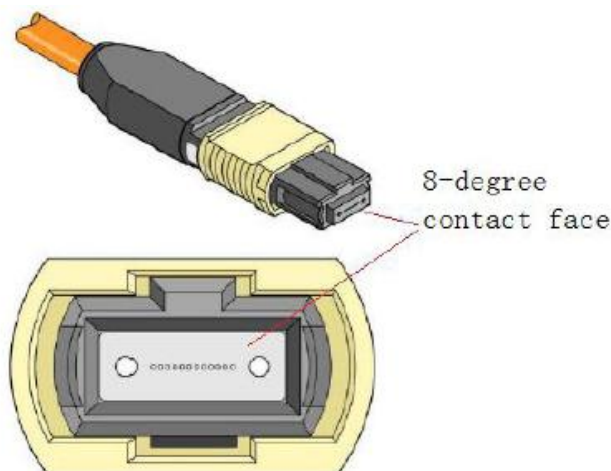
The optical interface port is a male MPO connector .The four fiber positions on the left as shown in Figure 2, with the key up, are used for the optical transmit signals (Channel 1 through4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.



Transmit Channels: 1 2 3 4  
 Unused positions: x x x x  
 Receive Channels: 4 3 2 1

**Figure 6. Optical Receptacle and Channel Orientation**

**Attention:** To minimize MPO connection induced reflections, an MPO receptacle with 8-degree angled end face is utilized for this product. A female MPO connector with 8-degree end-face should be used with this product as illustrated in Figure7



**Figure 7. Female MPO Connector with 8-degree End-face**

## ESD

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007)

## Order Information

The product part number for selected standard lengths is listed below.

Part Number	Product Description
QSFP-LR4-PSM	QSFP+ LR4 PSM 10km optical transceiver with full real-time digital diagnostic monitoring and pull tab

## Revision History

Revision	Initiated	Review	Approved	Revision History	Release Date
V1.0	Vinson	Steven	Nicky	Released.	Jun,30, 2016

## Further Information

For further information, please contact [info@10gtek.com](mailto:info@10gtek.com)

Tel : +86 755 2998 8100

Fax: +86 755 6162 4140

Web: www.10gtek.com