QSFP-DD Specification

for

QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER

Rev 2.0 March 13, 2017

Abstract: This specification defines: the electrical and optical connectors, electrical signals and power supplies, mechanical and thermal requirements, and the management interface of the pluggable QSFP Double Density (QSFP- DD) module, connector and cage system. This document provides a common specification for systems manufacturers, system integrators, and suppliers of modules.

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Foreword

The development work on this specification was done by the QSFP-DD MSA, an industry group. The membership of the committee since its formation in Feb 2016 has included a mix of companies which are leaders across the industry.

TABLE OF CONTENTS

1. Scope 7

1.1 Description of Sections *7*

2. References 7

2.1 Industry Documents *7*

2.2 Sources *7*

3 Introduction 8

3.1 Objectives *8*

3.2 Applications *9*

4 Electrical Specification 9

4.1 Electrical Connector *9*

4.1.1 Low Speed Electrical Hardware Signals 17

4.1.2 Low Speed Electrical Specification 18

4.1.3 High Speed Electrical Specification 19

4.2 Power Requirements *20*

4.2.1 Power Classes and Maximum Power Consumption 20

4.2.2 Host Board Power Supply Filtering 21

4.2.3 Module Power Supply Specification 21

4.2.4 Host Board Power Supply Noise Output 22

4.2.5 Module Power Supply Noise Output 22

4.2.6 Module Power Supply Noise Tolerance 22

4.3 ESD *24*

5 Mechanical and Board Definition 25

5.1 Introduction *25*

5.2 Datums, Dimensions and Component Alignment *26*

5.3 Module Mechanical Dimensions *28*

5.4 Module Flatness and Roughness *33*

5.5 Module paddle card dimensions *34*

5.6 Module Extraction and Retention Forces *37*

5.7 2x1 Electrical Connector Mechanical *38*
5.7.1 2x1 Connector and Cage host PCB layout 43

5.8 Surface Mount Electrical Connector Mechanical *45*
5.8.1 Surface mount connector and cage host PCB layout 52

5.9 Module Color Coding and Labeling *54*

5.10 Optical Interface *55*
5.10.1 MPO Optical Cable connections 56
5.10.2 Dual LC Optical Cable connection 58
5.10.3 Dual CS Optical Cable connection 58
5.10.4 Electrical data input/output to optical port mapping 59

6 Environmental and Thermal 59

6.1 Thermal Requirements *59*

7 Management Interface 60

7.1 Timing Specification *60*
7.1.1 Introduction 60
7.1.2 Management Interface Timing Specification 60
7.1.3 Serial Interface Protocol 61

7.2 Memory Interaction Specifications *63*
7.2.1 Timing for Soft Control and Status Functions 65

7.3 QSFP-DD Initialization State Machine *67*
7.3.1 MgmtInit State 68
7.3.2 MgmtReady State 69
7.3.3 DataPathInit State 69
7.3.4 DataPathPowered State 70
7.3.5 DataPathDeinit State 70
7.3.6 Reset State 71
7.3.7 Interrupt Flag Applicability Per State 71

7.4 QSFP-DD Memory Map *72*
7.4.1 Lower Page 00h 74
7.4.2 Upper Page 00h 87
7.4.3 Upper Page 01h 99
7.4.4 Upper Page 02h 100
7.4.5 Upper Page 03h 100

Table 1- Pad Function Definition..... 13
Table 2- Low Speed Control and Sense Signals..... 19
Table 3- Power Classification..... 20
Table 4- Power Supply specifications, Instantaneous, sustained and steady state current limits..... 23
Table 5- Datums..... 26
Table 6- Module flatness specifications..... 33
Table 7- Insertion, Extraction and Retention Forces..... 37
Table 8- Electrical data input to Optical Port Mapping..... 59
Table 9- Temperature Range Class of operation..... 59
Table 10- Management Interface timing parameters..... 62
Table 11- QSFP-DD Memory Specification..... 63
Table 12- Writable Memory Blocks..... 64
Table 13- Timing for QSFP-DD soft control and status functions..... 65
Table 14- I/O Timing for Squelch & Disable..... 66
Table 15- Interrupt Flag Classes..... 71
Table 16- Lower Page Overview (Lower Page)..... 74
Table 17- Identifier and Status Summary (Lower Page)..... 74
Table 18- Interrupt Flags (Lower Page, active modules only)..... 75
Table 19- State Indicators (Lower Page, active modules only)..... 77
Table 20- Channel State register encoding..... 78
Table 21- Module Monitors (Lower Page, active modules only)..... 78
Table 22- Channel Monitors (Lower Page, active modules only)..... 79
Table 23- Control Fields (Lower Page, active modules only)..... 80
Table 24- Tx Input Equalization..... 82
Table 25- Rx Output Pre-emphasis..... 82
Table 26- Rx Output Amplitude..... 83
Table 27- Interrupt Masks (Lower Page, active modules only)..... 83
Table 28- Upper Page 0 Overview (Page 00h)..... 87
Table 29- Identifiers (Page 00h)..... 88
Table 30- Specification compliance (Page 00h)..... 89
Table 31- Extended Rate Select compliance (Page 00h)..... 90
Table 32- Link Length (Page 00h)..... 90
Table 33- Device technology (Page 00h)..... 91
Table 34- Technology values..... 91
Table 35- Extended module code (Page 00h)..... 92
Table 36- Options (Page 00h)..... 94
Table 37- Diagnostic Monitoring Type (Page 00h)..... 95
Table 38- Enhanced Options (Page 00h)..... 96
Table 39- Device Properties (Page 00h)..... 97
Table 40- State Duration Encoding..... 99
Table 41- Application Table Header (Page 01h, active modules only)..... 99
Table 42- Legacy Table Entry (Page 01h, active modules only)..... 100
Table 43- Extended Table Entry (Page 01h, active modules only)..... 100
Table 44- Upper Page 3 Overview (Page 03h)..... 100
Table 45- Module Thresholds (Page 03h, active modules only)..... 101
Table 46- Channel Thresholds (Page 03h, active modules only)..... 102
Table 47- Extended Channel Controls (Page 03h, active modules only)..... 104
Table 48- Hardware/Firmware ID (Page 03h, active modules only)..... 106

Figure 1: Application Reference Model..... 9
Figure 2: Module pad layout..... 12
Figure 3: Example QSFP-DD Host Board Schematic For Optical Modules..... 15
Figure 4: Example QSFP-DD Host Board Schematic for active copper cables..... 16
Figure 5: Example QSFP-DD Host Board Schematic for passive copper cables..... 17
Figure 6: Recommended Host Board Power Supply Filtering..... 21
Figure 7: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)..... 22
Figure 8: 2x1 stacked cage and module..... 25
Figure 9: Press fit cage for surface mount (SMT) connector..... 25
Figure 10: Pluggable module..... 26
Figure 11: 2X1 stacked connector/cage datum descriptions..... 27
Figure 12: Surface mount connector/cage datum descriptions..... 28
Figure 13: Module..... 29
Figure 14: Drawing of module..... 30
Figure 15: Detailed dimension of module..... 32
Figure 16: Module paddle card dimensions..... 35
Figure 17: Module pad dimensions..... 36
Figure 19: 2x1 stacked cage..... 39
Figure 20: 2x1 stacked cage dimensions..... 40
Figure 21: Connector pins in 2x1 stacked cage as viewed from the front..... 41
Figure 22: 2x1 Bezel Opening..... 42
Figure 23: 2X1 host board connector contacts..... 43
Figure 24: 2X1 Host PCB Mechanical Layout..... 45
Figure 25: SMT connector in 1xn cage..... 46
Figure 26: SMT 1x1 Cage Design..... 48
Figure 27: SMT 1x1 Connector Design..... 50
Figure 28: SMT 1xn bezel opening..... 51
Figure 29: SMT Host PCB Mechanical Layout..... 52
Figure 30: SMT Connector and Host PCB Pin Numbers..... 53
Figure 31: Optical Media Dependent Interface port assignments..... 55
Figure 32: MPO-12 Single Row optical patch cord and module receptacle..... 56
Figure 33: MPO-16 Single Row optical patchcord and module receptacle..... 57
Figure 34: MPO-12 Two Row optical patchcord and module receptacle..... 57
Figure 35: Dual LC optical patchcord and module receptacle..... 58
Figure 36: Dual CS connector module receptacle (in support of breakout applications)... 58
Figure 37: QSFP-DD Timing Diagram..... 61
Figure 38: SDA and SCL tradeoffs options for pull-up resistor, bus capacitance and rise/fall times..... 63
Figure 39 Initialization State Machine..... 67
Figure 40: QSFP-DD Memory Map..... 73

QSFP-DD 8X Pluggable Transceiver

1. Scope

The scope of this specification is the definition of a high density 8-channel (8x) module, cage and connector system. QSFP-DD supports up to 400 Gb/s in aggregate over an 8 x 50 Gb/s electrical interface. The cage and connector design provides backwards compatibility to QSFP28 modules which can be inserted into a QSFP-DD port and connected to 4 of the 8 electrical channels.

1.1 Description of Sections

Section 1 Scope and Purpose

Section 2 Referenced and Related Standards and SFF Specifications

Section 3 Introduction

Section 4 Electrical specifications

Section 5 Mechanical specifications and printed circuit board recommendations

Section 6 Environmental and thermal considerations

Section 7 Management interface, initialization and management register contents.

2. References

2.1 Industry Documents

The following interface standards and specifications are relevant to this Specification.

- GR-253-CORE
- IEEE Std 802.3
- IEEE Std 802.3by
- IEEE Std 802.3bs
- IEEE Std 802.3cd
- InfiniBand Architecture Specifications
- FC-PI-6p
- FC-PI-7

SFF Specifications

- INF-8436 QSFP (Quad SFP) 4 Gbps 4X Transceiver
- SFF-8636 Shielded Cables Common Management Interface
- SFF-8472 Diagnostic Monitoring Interface for Optical Transceivers
- SFF-8661 QSFP+ 4X Pluggable Module
- SFF-8679 QSFP28 4X Base Electrical Specification

CS optical connector specification

- CS-01242017 Can be found at www.QSFP-DD.com

2.2 Sources

This document can be obtained via the www.QSFP-DD.com web site.

3 Introduction

This Specification covers the following items:

a) Electrical interfaces including pad assignments for data, control, status and power supplies and host PCB layout requirements.

b) Management interface encompassing features from SFF-8636 with extensions for 8x electrical channels and 400Gb/s data path.

c) Optical interfaces (including optical receptacles and mating fiber plugs for multimode and single-mode duplex and parallel fiber applications). Breakout cable applications are also specified. Optical signaling specifications are not included in this document but are defined in the applicable industry standards.

d) Mechanical specifications including dimensions and tolerances for the connector, cage and module system. Includes details of the requirements for correct mating of the module and host sides of the connector.

e) Thermal requirements

f) Electrostatic discharge (ESD) requirements by reference to industry standard limits and test methods.

This Specification does not cover the following items:

a) Electromagnetic interference (EMI) protection. EMI protection is the responsibility of the implementers of the cages and modules.

3.1 Objectives

Electrical signal contact and channel assignments, electrical and power requirements defined in Section 4, optical lane assignments defined in Section 5 and the management interface requirements defined in Section 7 ensure that the pluggable modules and cable assemblies are functionally interchangeable. Dimensions, mounting and insertion requirements defined in Section 5 for the bezel, optical module, cable plug, cage and connector system on a circuit board ensure that these products are mechanically interchangeable.

3.2 Applications

This specification defines a common solution for combined eight-channel ports that support Ethernet and/or InfiniBand and/or Fibre Channel requirements. The QSFP-DD interface can support pluggable modules or direct attach cables based on multimode fiber, single mode fiber or copper wires.
An application reference Model, shown in Figure 1, shows the high-speed data interface between an ASIC and the QSFP-DD module.

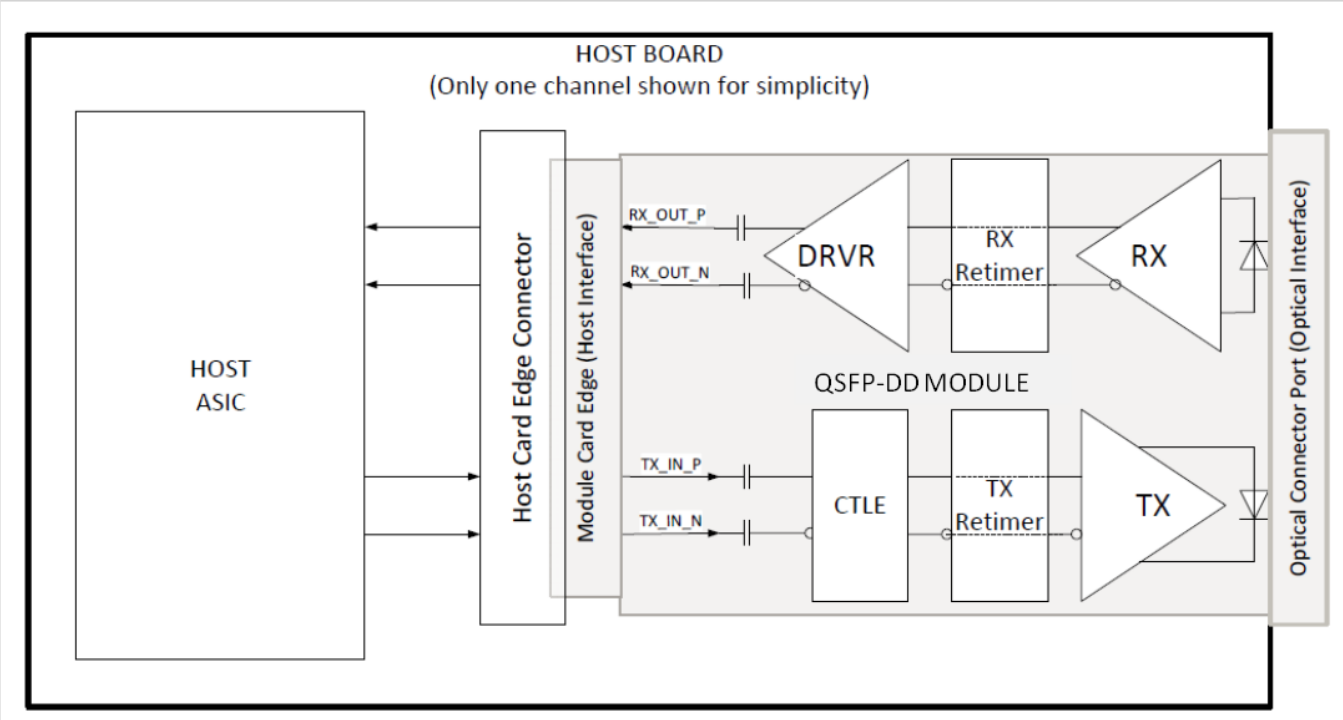


Figure 1: Application Reference Model

Note: For high speed electrical signals the compliance board methodology of IEEE and OIF should be used. Measurements taken with QSFP-DD compliance boards should be corrected for any difference between the loss of these compliance boards and the loss of the compliance boards specified in the standard.

4 Electrical Specification

This section contains signal definitions and requirements that are specific to the QSFP-DD module. High-speed signal requirements including compliance points for electrical measurements are defined in the applicable industry standard.

4.1 Electrical Connector

The QSFP-DD module edge connector consists of a single paddle card with 38 pads on the top and 38 pads on the bottom of the paddle card for a total of 76 pads. The pads are defined in such a manner so as to accommodate insertion of a QSFP module into a QSFP-DD receptacle. The legacy signal locations are deeper on the paddlecard, so that legacy QSFP module pads only connect to the longer row of connector pins, leaving the short row of connector pins open circuited in a QSFP application.

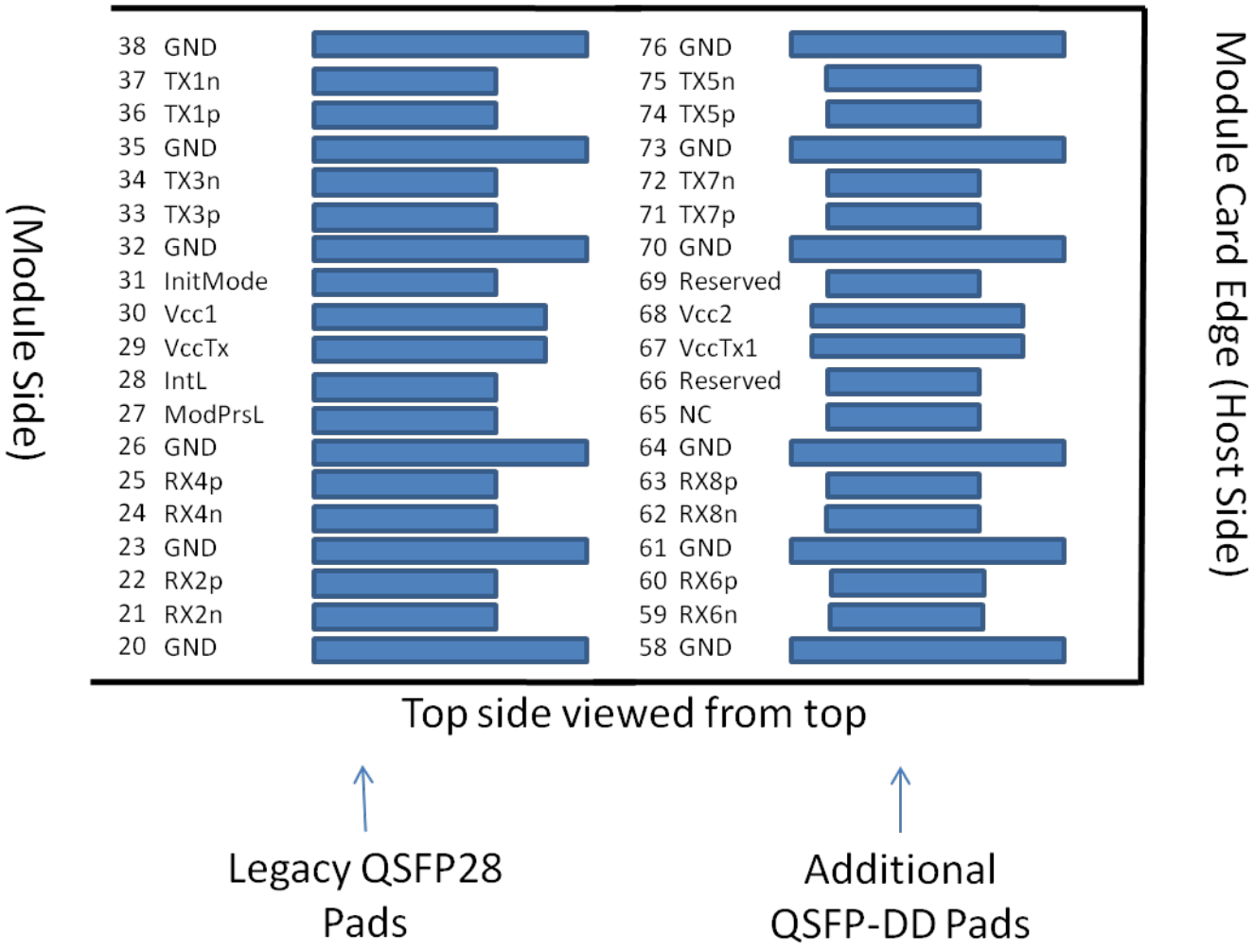
The pads are designed for a sequenced mating:

First mate – ground pads
Second mate – power pads
Third mate – signal pads

Because the QSFP-DD module has 2 rows of pads, the additional QSFP-DD pads will have an intermittent connection with the legacy QSFP pins in the connector during the module insertion and removal. The 'legacy' QSFP pads have a 'B' label shown in Table 1 to designate them as the second row of module pads to contact the QSFP-DD connector. The additional QSFP-DD pads have an 'A' label in Table 1 to designate them as the first row of module pads to contact the QSFP-DD connector. The additional QSFP-DD pads have first, second and third mate to the connector pins for both insertion and removal. Each of the first, second and third mate connections of the legacy QSFP pads and the respective additional QSFP-DD pads are simultaneous.

Figure 2 shows the signal symbols and pad numbering for the QSFP-DD module edge connector. The diagram shows the module PCB edge as a top and bottom view. There are 76 pads intended for high speed signals, low speed signals, power and ground connections. Table 1 provides more information about each of the 76 pads. Figure 16 and Figure 17 show pad dimensions . The connector can be integrated into a 2x1 stacked configuration with 2 ports as illustrated in Figure 8 or a surface mount configuration as shown in Figure 9.

For EMI protection the signals from the host connector should be shut off when the QSFP-DD module is not present. Standard board layout practices such as connections to Vcc and GND with vias, use of short and equal-length differential signal lines and 50 Ohm terminations are recommended. The chassis ground (case common) of the QSFP-DD module should be isolated from the module’s circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.


(Module Side)
38 GND
37 TX1n
36 TX1p
35 GND
34 TX3n
33 TX3p
32 GND
31 InitMode
30 Vcc1
29 VccTx
28 IntL
27 ModPrsL
26 GND
25 RX4p
24 RX4n
23 GND
22 RX2p
21 RX2n
20 GND
76 GND
75 TX5n
74 TX5p
73 GND
72 TX7n
71 TX7p
70 GND
69 Reserved
68 Vcc2
67 VccTx1
66 Reserved
65 NC
64 GND
63 RX8p
62 RX8n
61 GND
60 RX6p
59 RX6n
58 GND
Module Card Edge (Host Side)
Top side viewed from top
Legacy QSFP28 Pads
Additional QSFP-DD Pads

.

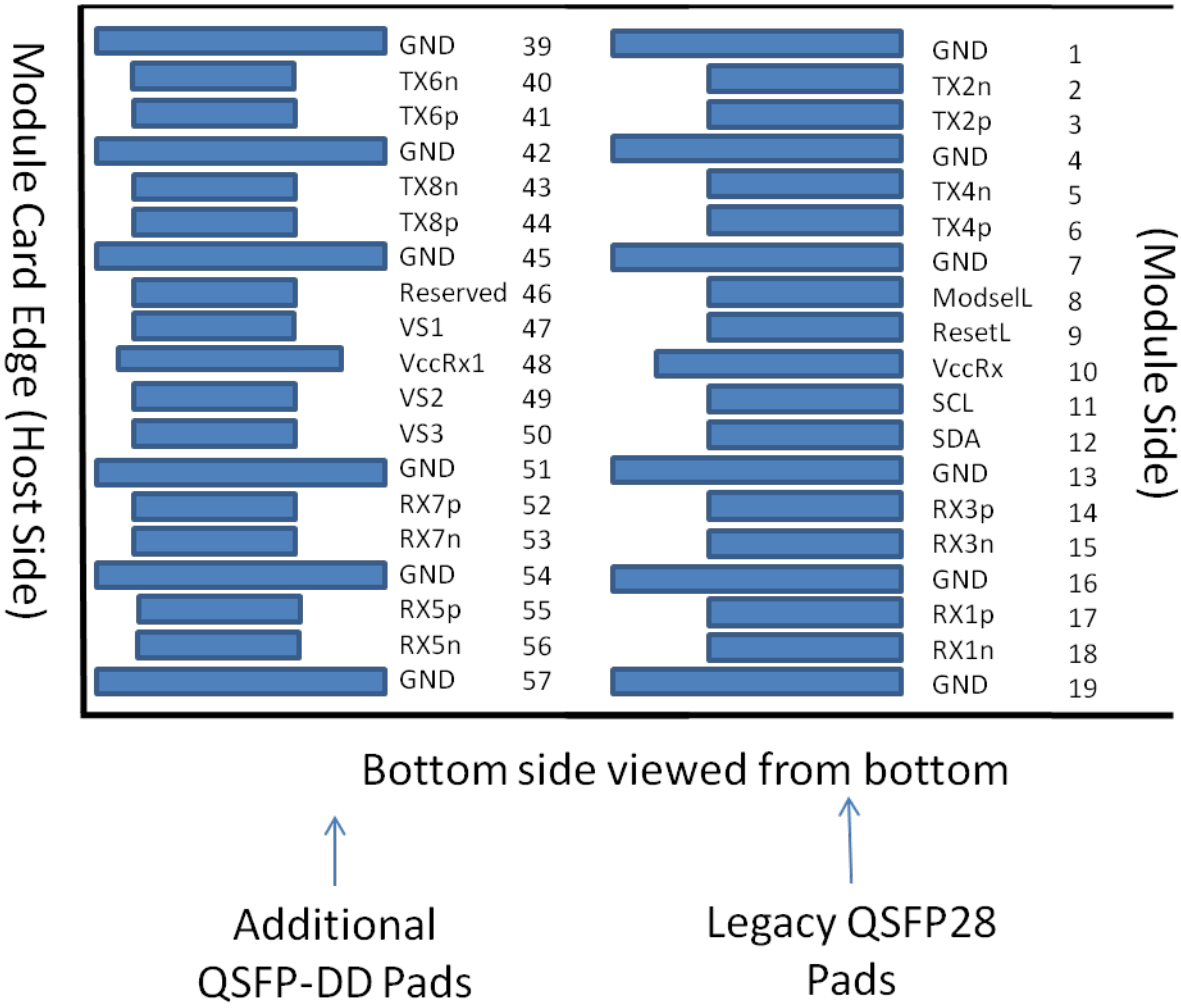


Figure 2: Module pad layout

Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Figure 3, Figure 4 and Figure 5 show examples of QSFP-DD host PCB schematics with connections to CDR and control ICs. An 8 wide electrical/optical interface is shown. Note alternate electrical/optical interfaces are supported using optical multiplexing (WDM) or electrical multiplexing.

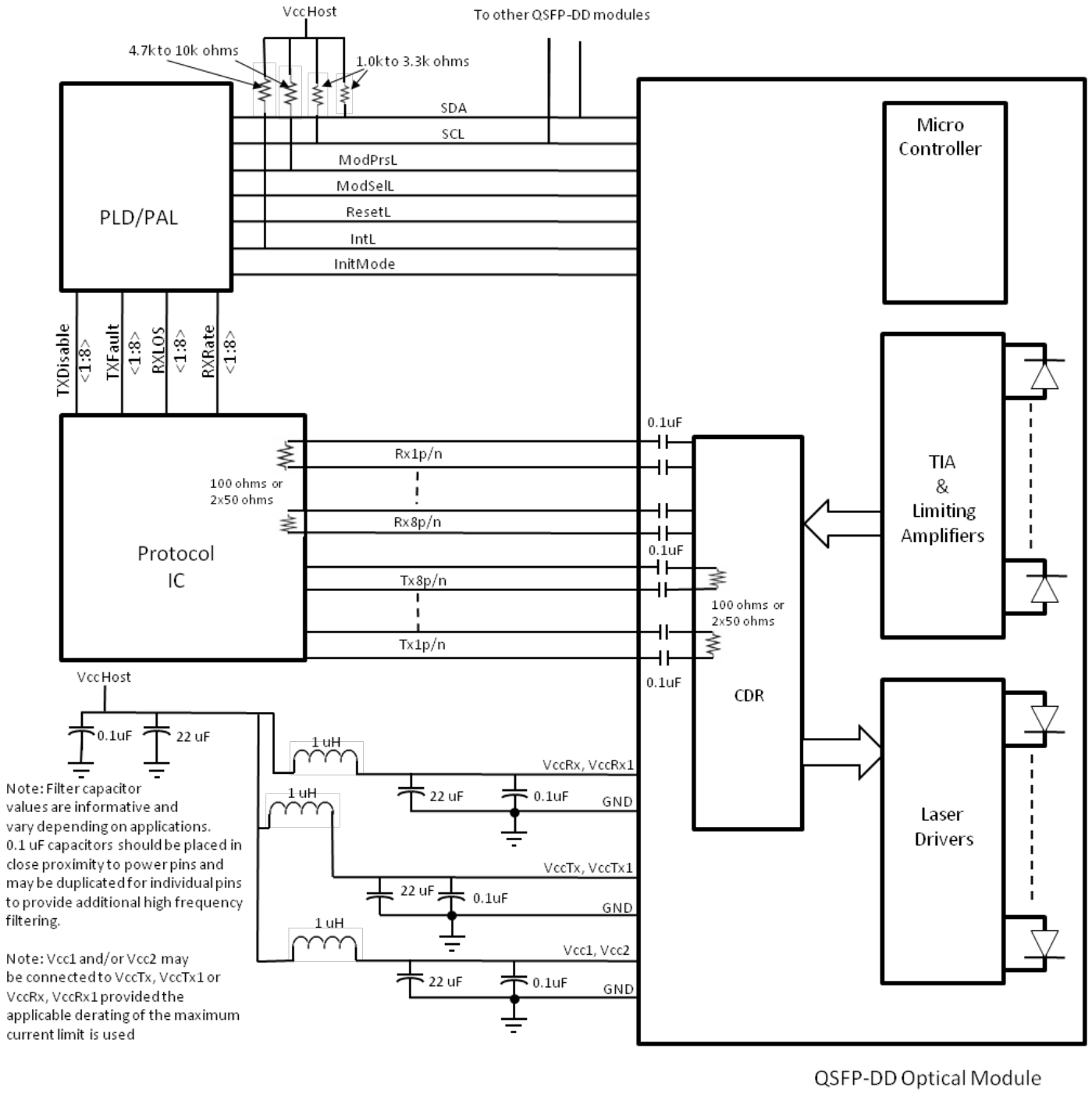


Figure 3: Example QSFP-DD Host Board Schematic For Optical Modules

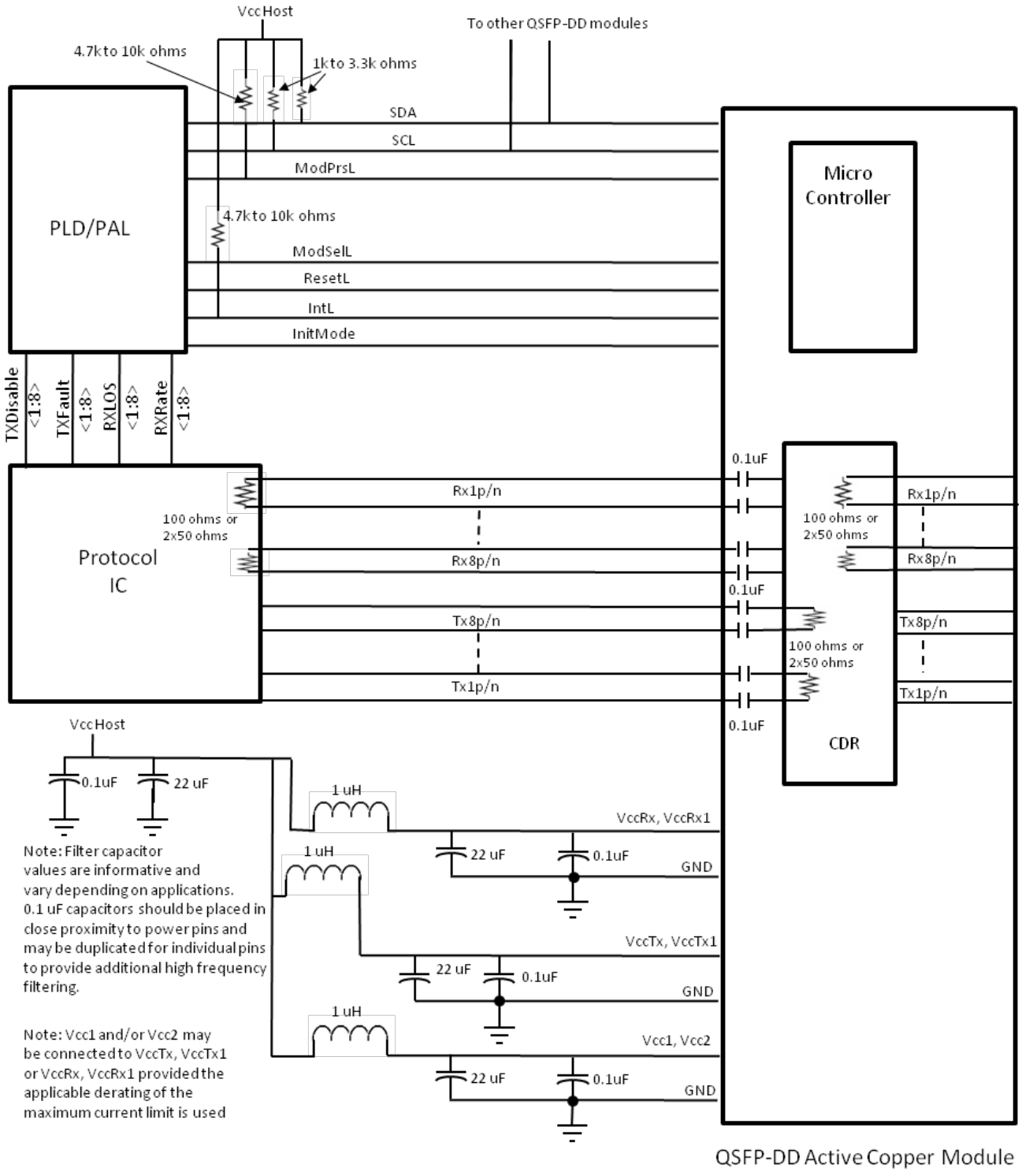


Figure 4: Example QSFP-DD Host Board Schematic for active copper cables

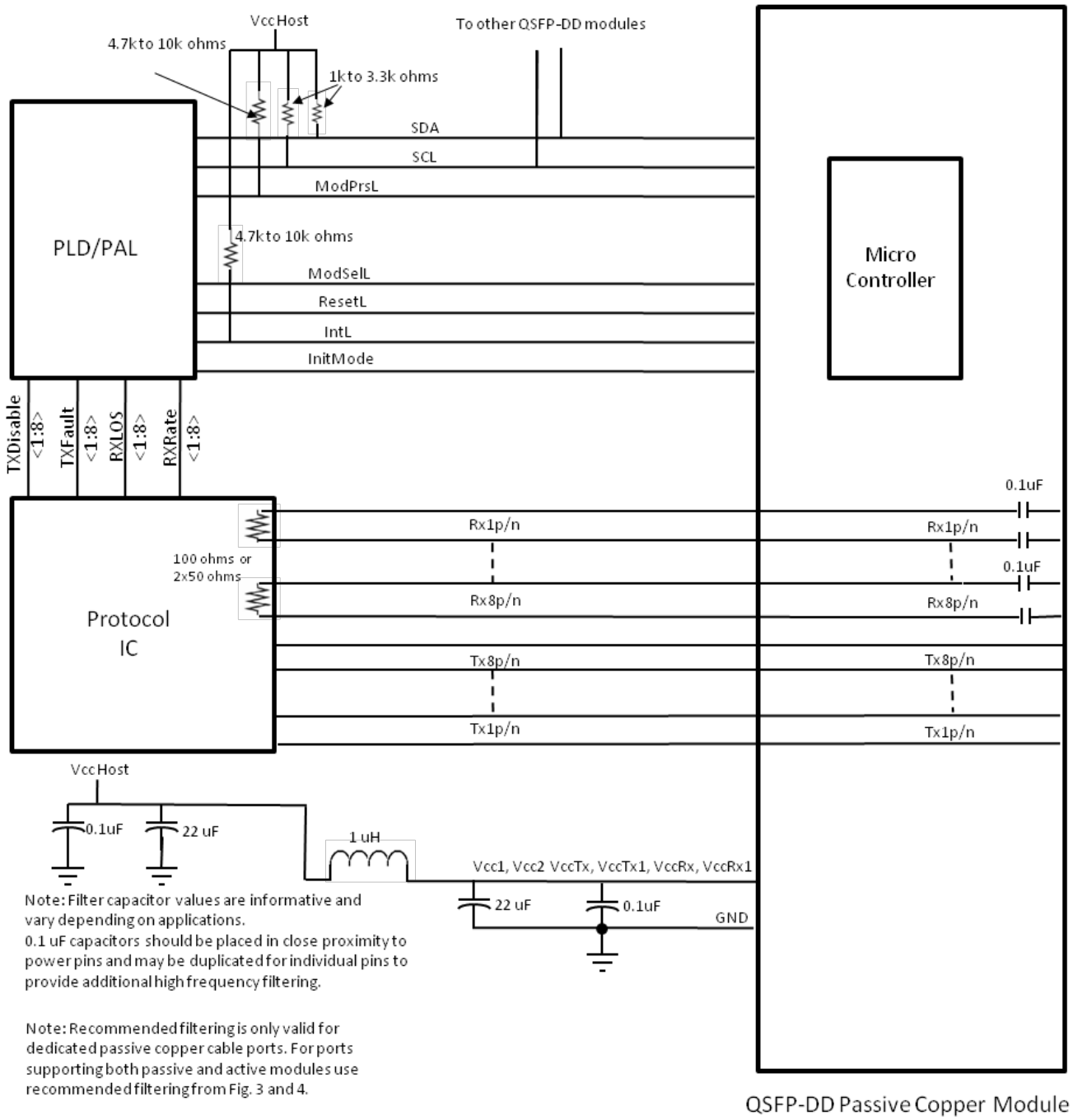


Figure 5: Example QSFP-DD Host Board Schematic for passive copper cables

4.1.1 Low Speed Electrical Hardware Signals

In addition to the 2-wire serial interface the module has the following low speed signals for control and status:

ModSelL
ResetL
InitMode
ModPrsL
IntL

4.1.1.1 ModSelL

The ModSelL is an input signal that must be pulled to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP-DD modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.1.1.2 ResetL

The ResetL signal shall be pulled to Vcc in the module. A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 13) initiates a complete module reset, returning all user module settings to their default state.

4.1.1.3 InitMode

InitMode is an input signal. The InitMode signal must be pulled up to Vcc in the QSFP-DD module. The InitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (InitMode asserted High) or module hardware control (InitMode deasserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in Section 7.5. Under hardware control (InitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for signal description.

4.1.1.4 ModPrsL

ModPrsL must be pulled up to Vcc Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

4.1.1.5 IntL

IntL is an output signal. The IntL signal is an open collector output and must be pulled to Vcc Host on the host board. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read.

4.1.2 Low Speed Electrical Specification

Low speed signaling other than the SCL and SDA interface is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc host on each of the 2-wire interface SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus.

Note: Timing diagrams for SCL and SDA are included in Section 7.1.2 Management Interface Timing Specification.

The QSFP-DD low speed electrical specifications are given in Table 2. This specification ensures compatibility between host bus masters and the 2-wire interface.

Table 2- Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms Pullup resistor, max
			200	pF	1.6 k Ohms pullup resistor max
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	|Iin|<=125 uA for 0V<Vin,Vcc
	VIH	2	VCC+0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	

4.1.3 High Speed Electrical Specification

For detailed electrical specifications see the appropriate specification, e.g. 802.3ba Annex 86A, 802.3bs Annex 120E, FC-PI-6, FC-PI-7, OIF-CEI-28G-VSR, OIF-CEI-56G-VSR or the InfiniBand specification.
Partial or complete squelch specifications may be provided in the appropriate specification. Where squelch is not fully defined by the appropriate specification, the recommendations of the following subsections 4.1.3.1 and 4.1.3.2 may be used.

4.1.3.1 Rx(n)(p/n)

Rx(n)(p/n) are QSFP-DD module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP-DD module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less.

Output squelch for loss of optical input signal, hereafter RX Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output as shown in Section 5.10.4. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp.

In normal operation the default case has RX Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

4.1.3.2 Tx(n)(p/n)

Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP-DD optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.

Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 50 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel,

the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.

For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch is an optional function. If TX squelch is implemented, the disable squelch must be provided.

4.2 Power Requirements

The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. Power is applied concurrently to these pins.

A host board together with the QSFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 4 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

4.2.1 Power Classes and Maximum Power Consumption

There are two power modes; Low Power Mode and High Power Mode. Modules are either in Low Power Mode or High Power Mode as defined in Table 4 and Section 7.
Since different classes of modules exist with pre-defined maximum power consumption limits, it is necessary to avoid exceeding the system power supply limits and cooling capacity when a module is inserted into a system designed to only accommodate lower power modules. It is recommended that the host implement the state machine recommended in Section 7 and identify the power class of the module before allowing the module to go into high power mode.

Power levels associated with classifications of modules are shown in Table 3.

Table 3- Power Classification

Power Class	Max Power (W)
1	1.0
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

In general, the higher power classification levels are associated with higher data rates and longer reaches. The system designer is responsible for ensuring that the maximum case temperature does not exceed the case temperature requirements.

4.2.2 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 6.

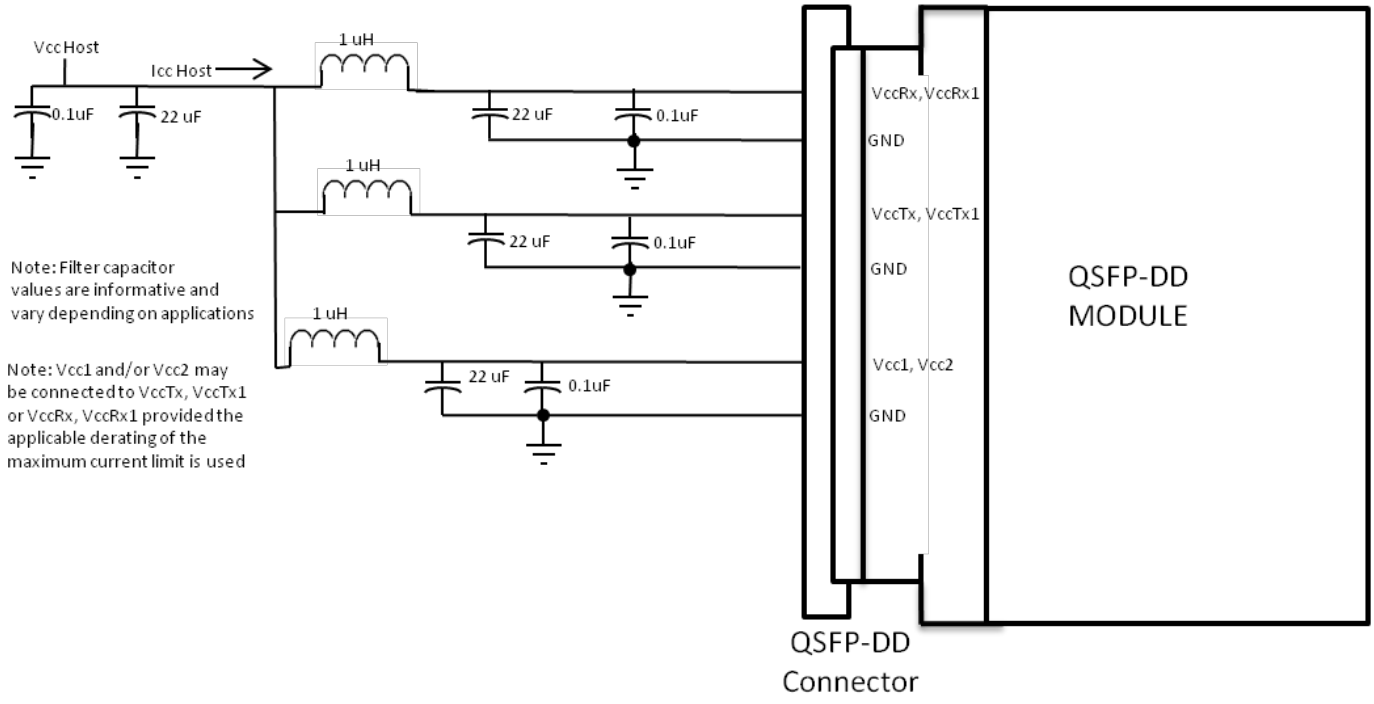


Figure 6: Recommended Host Board Power Supply Filtering

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 Ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 uF capacitors each have an equivalent series resistance of 0.22 ohm.

The specifications for the power supply are shown in Table 4. The limits in Table 4 apply to the combined current that flows through all inductors in the power supply filter (represents ICC host in Figure 6). The test method for measuring inrush current can be found in http://cp.literature.agilent.com/litweb/pdf/5991-2778EN.pdf.

4.2.3 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP-DD modules shall power up in Low Power Mode if InitMode is asserted. If InitMode is not asserted the module will proceed to High Power Mode without host intervention. Figure 7 shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes. Specification values for maximum instantaneous, sustained and steady state currents at each power class are given in Table 4.

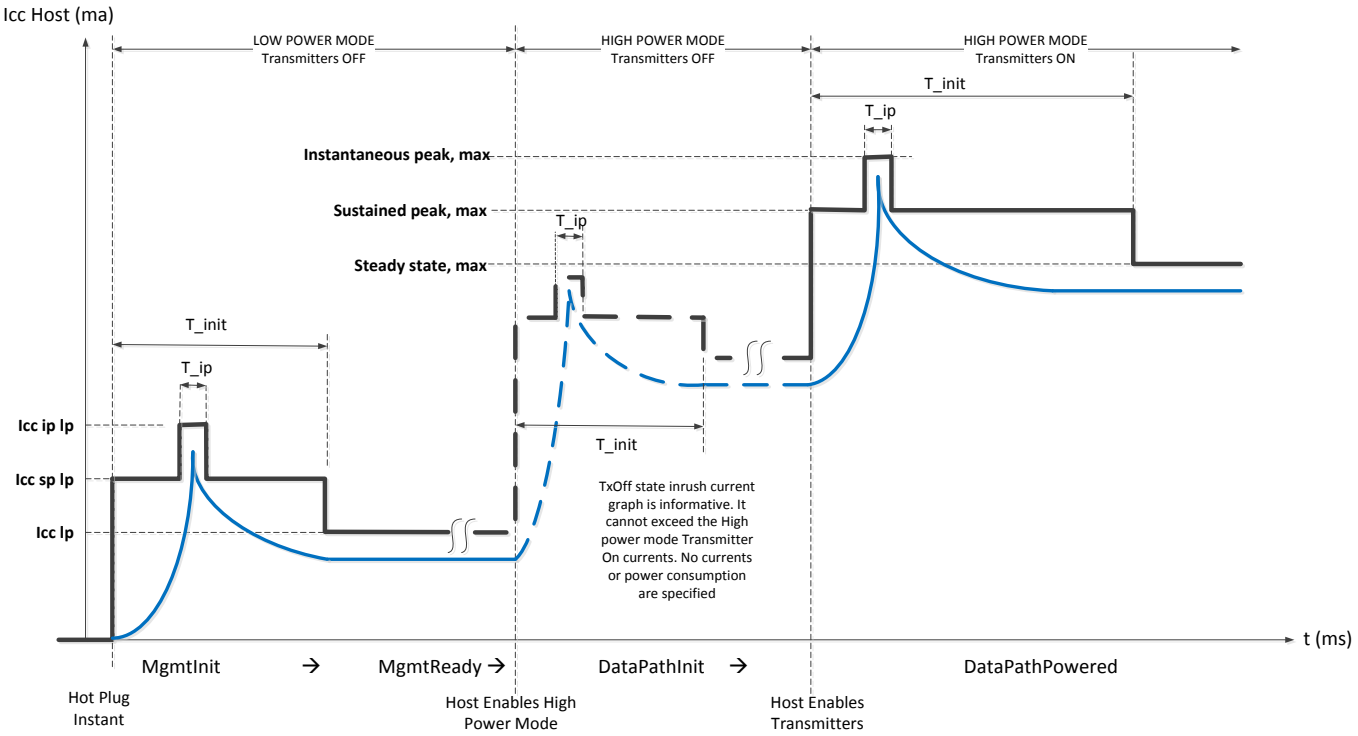


Figure 7: Instantaneous and sustained peak currents for Icc Host (see Fig. 6)

4.2.4 Host Board Power Supply Noise Output

The host shall generate an effective weighted integrated spectrum RMS noise less than the value in Table 4 when tested by the methods of SFF-8431, section D.17.1.

4.2.5 Module Power Supply Noise Output

The QSFP-DD module shall generate less than the value in Table 4 when tested by the methods of SFF-8431, section D.17.2. Note: The series resister specified in D.17 Figure 56 may need to be reduced for high power modules.

4.2.6 Module Power Supply Noise Tolerance

The QSFP-DD module shall meet all requirements and remain fully operational in the presence of a sinusoidal tolerance signal of amplitude given by Table 4, swept from 10 Hz to 10 MHz according to the methods of SFF-8431, section D.17.3. This emulates the worst case noise output of the host.

Table 4- Power Supply specifications, Instantaneous, sustained and steady state current limits

Parameter	Symbol	Min	Nom	Max	Unit
Power supply voltages VccTx, VccTx1, VccRx, VccRx1, Vcc1 & Vcc2 including ripple, droop and noise below 100kHz[1]		3.135	3.3	3.465	V
Host RMS noise output 10 Hz-10 MHz				25	mV
Module RMS noise output 10 Hz - 10 MHz				15	mV
Module power supply noise tolerance 10 Hz - 10 MHz (peak-to-peak)	$PSNR_{mod}$			66	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Low Power Mode[2]					
Power Consumption	P_lp			1.0	W
Instantaneous peak current at hot plug	Icc_ip_lp	-	-	400	mA
Sustained peak current at hot plug	Icc_sp_lp	-	-	330	mA
Steady state current	Icc_lp	-	-	288	mA
Power Class 1 module					
Power Consumption	P_1			1.0	W
Instantaneous peak current	Icc_ip_1	-	-	400	mA
Sustained peak current	Icc_sp_1	-	-	330	mA
Steady state current	Icc_1	-	-	288	mA
Power Class 2 module					
Power Consumption	P_2			3.5	W
Instantaneous peak current	Icc_ip_2	-	-	1400	mA
Sustained peak current	Icc_sp_2	-	-	1155	mA
Steady state current	Icc_2	-	-	1010	mA
Power Class 3 module					
Power Consumption	P_3			7	W
Instantaneous peak current	Icc_ip_3	-	-	2800	mA
Sustained peak current	Icc_sp_3	-	-	2310	mA
Steady state current	Icc_3	-	-	2020	mA
Power Class 4 module					
Power Consumption	P_4			8	W
Instantaneous peak current	Icc_ip_4	-	-	3200	mA
Sustained peak current	Icc_sp_4	-	-	2640	mA
Steady state current	Icc_4	-	-	2308	mA
Power Class 5 module					
Power Consumption	P_5			10	W
Instantaneous peak current	Icc_ip_5	-	-	4000	mA
Sustained peak current	Icc_sp_5	-	-	3300	mA
Steady state current	Icc_5	-	-	2886	mA
Power Class 6 module					
Power Consumption	P_6			12	W
Instantaneous peak current	Icc_ip_6	-	-	4800	mA
Sustained peak current	Icc_sp_6	-	-	3960	mA
Steady state current	Icc_6	-	-	3463	mA
Power Class 7 module					
Power Consumption	P_7			14	W
Instantaneous peak current	Icc_ip_7	-	-	5600	mA
Sustained peak current	Icc_sp_7	-	-	4620	mA
Steady state current	Icc_7	-	-	4040	mA
Power Class 8 module					
Power Consumption	P_8[3]			>14	W
Instantaneous peak current	Icc_ip_8	-	-	P_8/2.5	A
Sustained peak current	Icc_sp_8	-	-	P_8/3.03	A
Steady state current	Icc_8	-	-	P_8/3.465	A

Note 1: Measured at VccTx, VccTx1, VccRx, VccRx1, Vcc1 and Vcc2
Note 2: Host designers are responsible for handling 1.5W Low Power Mode QSFP legacy modules as appropriate in their system.
Note 3: User must read register 229 for maximum power consumption

4.3 ESD

Where ESD performance is not otherwise specified, e.g. in the InfiniBand specification, the QSFP-DD module shall meet ESD requirements given in EN61000-4-2, criterion B test specification when installed in a properly grounded cage and chassis. The units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case. All the QSFP-DD module and host pins including high speed signal pins shall withstand 1000 V electrostatic discharge based on Human Body Model per ANSI/ESDA/JEDEC JS-001.

5 Mechanical and Board Definition

5.1 Introduction

The cages and modules defined in this section are illustrated in Figure 8 (2x1 stacked cage), Figure 9 (surface mount cage) and Figure 10 (pluggable module). All Pluggable modules and direct attach cable plugs must mate to the connectors and cages defined in this specification. Heat sink/clip thermal designs are application specific and not specifically defined by this specification.

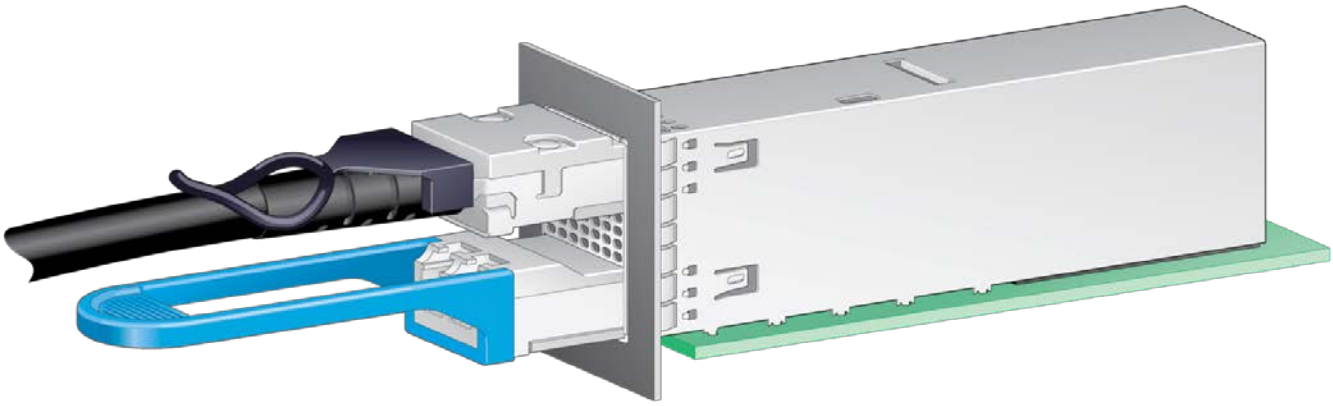


Figure 8: 2x1 stacked cage and module

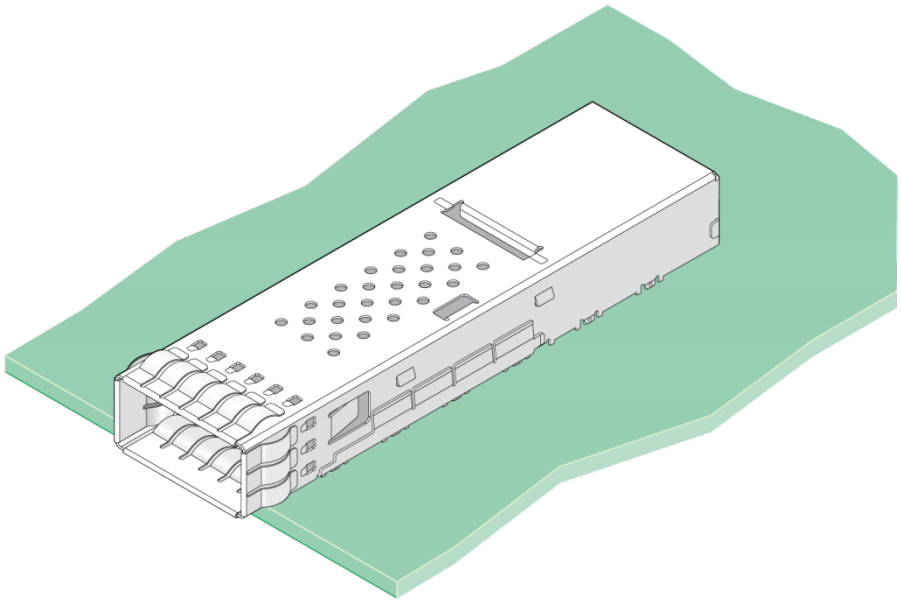


Figure 9: Press fit cage for surface mount (SMT) connector

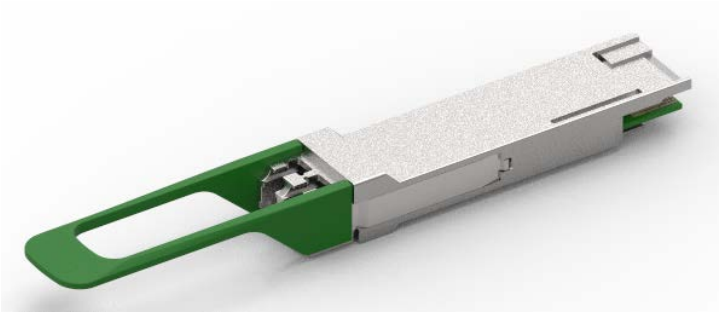


Figure 10: Pluggable module

5.2 Datums, Dimensions and Component Alignment

A listing of the datums for the various components is contained in Table 5. The alignments of some of the datums are noted. In order to reduce the complexity of the drawings, all dimensions are considered centered unless otherwise specified. Dimensions and tolerancing conform to ASME Y14.5-2009. All dimensions are in millimeters.

Table 5- Datums

Datum	Description
A	Host Board Top Surface
B	Inside surface of bezel
C	**Distance between Connector terminal thru holes on host board
D	*Hard stop on module
E	**Width of module
F	Height of module housing
G	**Width of module pc board
H	Leading edge of signal contact pads on module pc board
J	Top surface of module pc board
K	*Host board thru hole #1 to accept connector guide post
L	*Host board thru hole #2 to accept connector guide post
M	**Width of bezel cut out
N	*Connector alignment pin
S	Seating plane of cage on host board
T	*Hard stop on cage
X & Y	Host board horizontal and depth datums
AA	**Connector slot width
BB	Seating plane of cage on host board
DD	Top surface of connector backshell
EE	Centerline of module opening to locate paddle card Datum H
*Datums D, N and T are aligned when assembled (see Figure 11 and Figure 12) **Centerlines of datums AA, C, E, G, M are aligned on the same vertical plane	

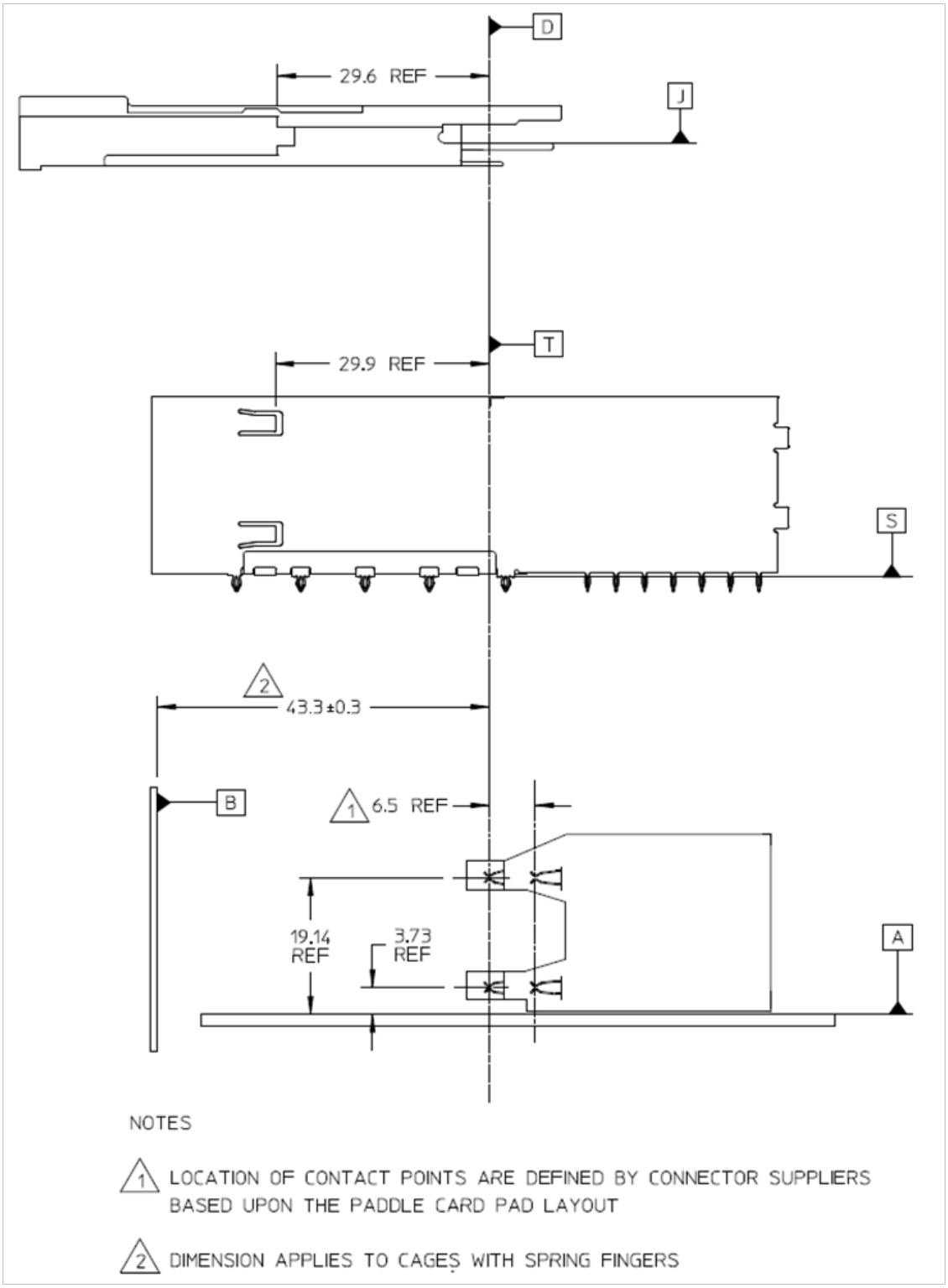


Figure 11: 2X1 stacked connector/cage datum descriptions

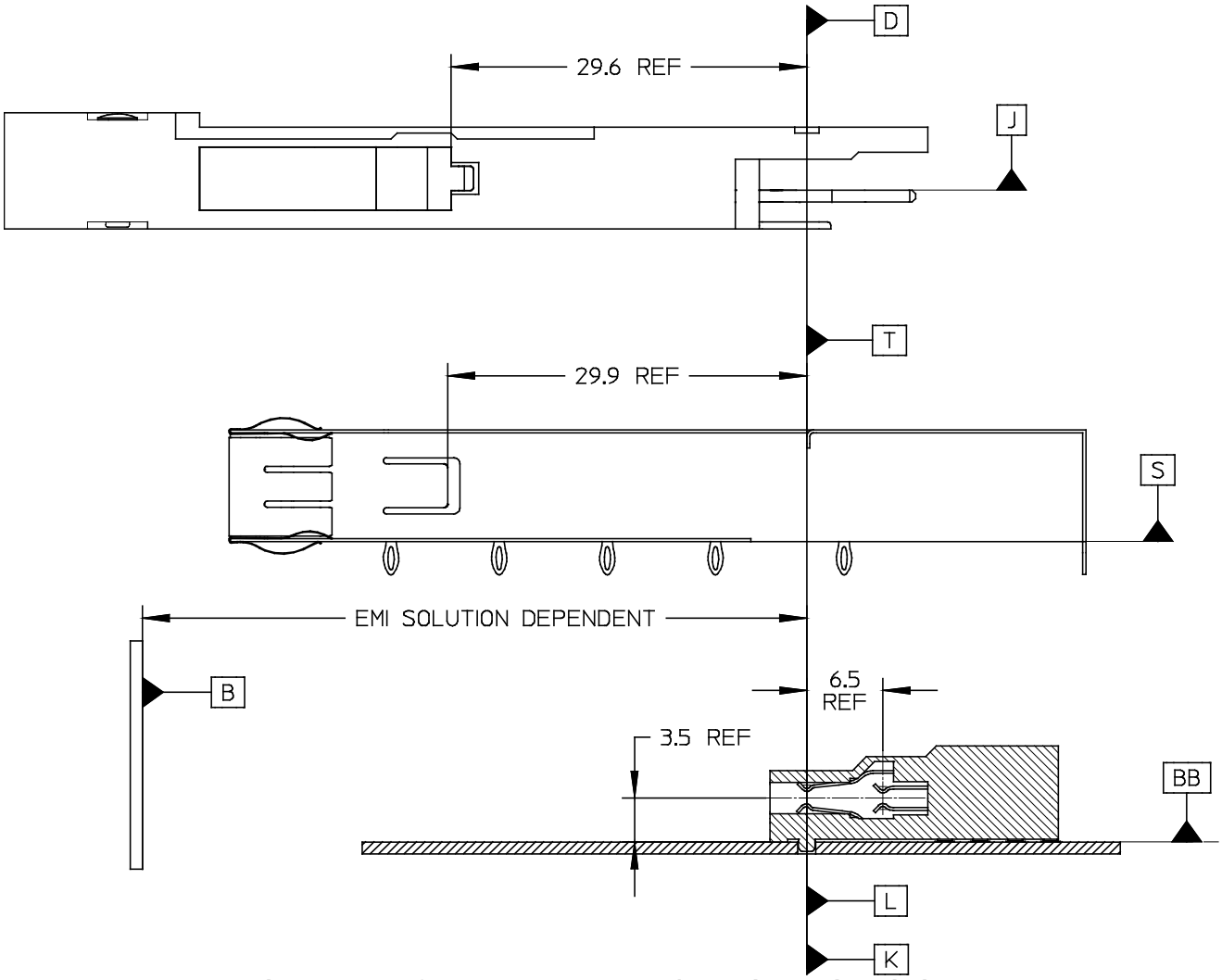


Figure 12: Surface mount connector/cage datum descriptions

5.3 Module Mechanical Dimensions

The mechanical outline for the QSFP-DD module and direct attach cables is shown in Figure 13, Figure 14 and Figure 15. The module shall provide a means to self-lock with either the 2x1 stacked cage or SMT cage upon insertion. The module package dimensions are defined in Figure 14 and Figure 15. The dimensions that control the size of the module that extends outside of the cage are listed as maximum dimensions per Note 4 in Figure 14. Note: All dimensions are in mm.

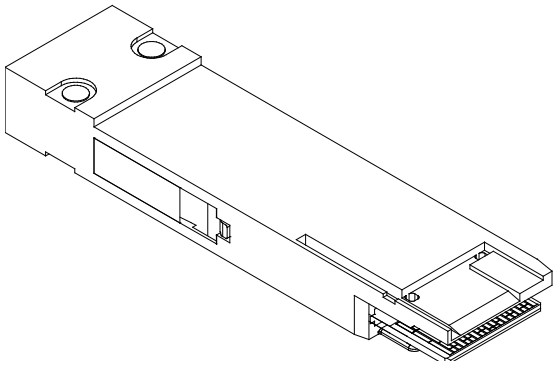


Figure 13: Module

NOTES APPLY TO MODULE DRAWINGS :

1. DIMENSIONS AND TOLERANCING CONFORM TO ASME Y14.5-2009.

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. SHARP CORNERS AND EDGES ARE NOT ALLOWED. ROUND OFF ALL EDGES AND CORNERS TO A MINIMUM RADUS OF 0.10 MM.

4 DIMENSION DEFINES ENLARGED SECTION OF TRANSCEIVER THAT EXTENDS OUTSIDE OF CAGE TO ACCOMMODATE MATING PLUG AND ACTUATOR MECHANISM.

5 SURFACES ON ALL 4 SIDES OF THE 12.4 MIN DIMENSION TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

6 DIMENSION APPLIES TO LATCH MECHANISM.

7 DIMENSION APPLIES TO THE LOCATION OF THE EDGE OF THE MODULE BOARD PAD, DATUM H, CONTACTS 21, 22, 36 AND 37 ARE VISIBLE.

8 DIMENSION TO INCLUDE BAIL TRAVEL.

9 DIMENSIONS APPLY TO OPENINGS IN THE HOUSING.

10 OPTIONAL FEATURE TO AID INSPECTION OF DIMENSIONS FROM DATUM D.

11 FLATNESS AND SURFACE ROUGHNESS (Ra) APPLIES FOR INDICATED LENGTH AND MIN WIDTH OF 13 MM. SURFACE TO BE THERMALLY CONDUCTIVE. SEE SECTION 5.4 TABLE 6 FOR FLATNESS AND ROUGHNESS REQUIREMENTS.

12 HIGHER WATTAGE MODULES MAY REQUIRE ADDITIONAL SPACE FOR COOLING.

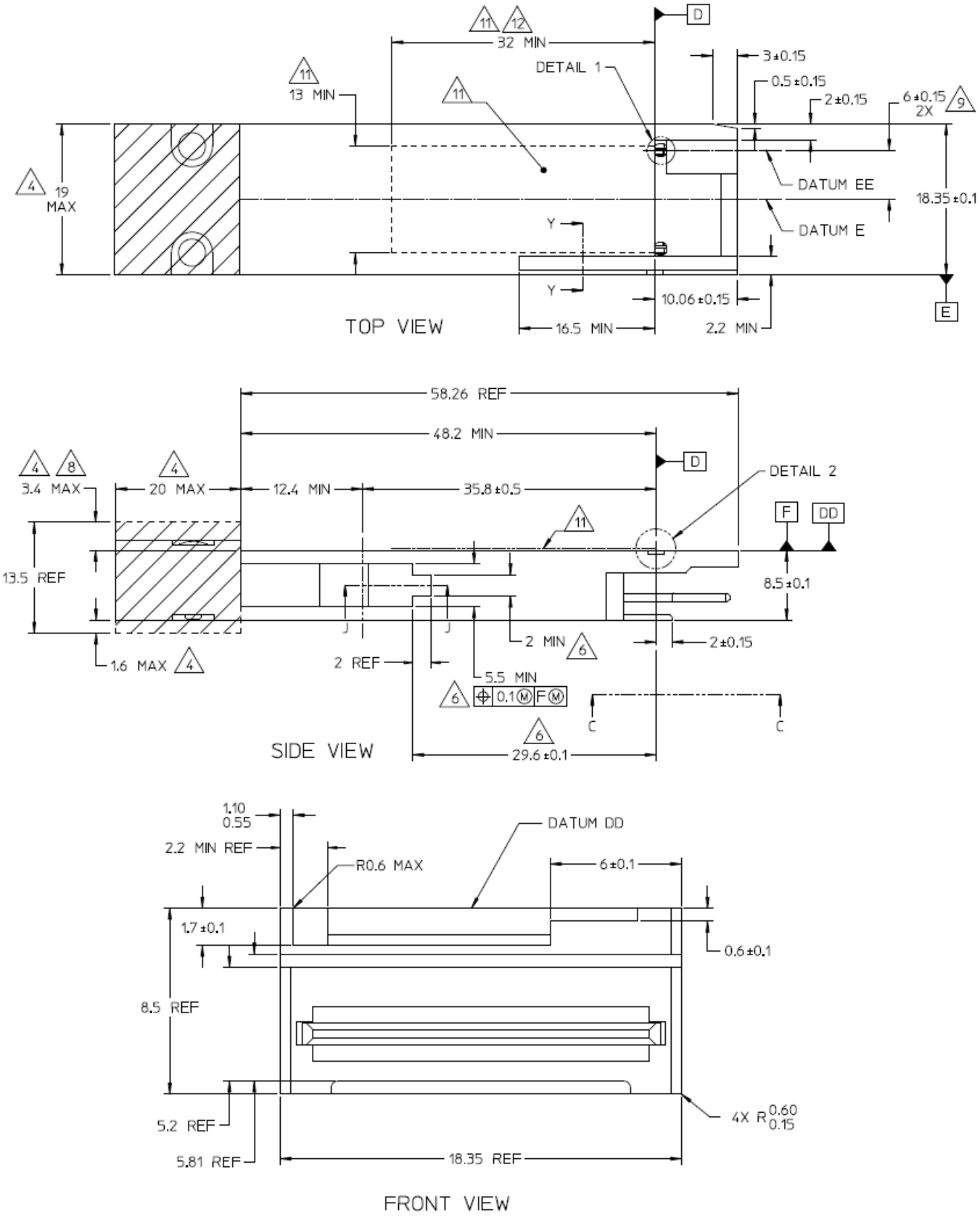
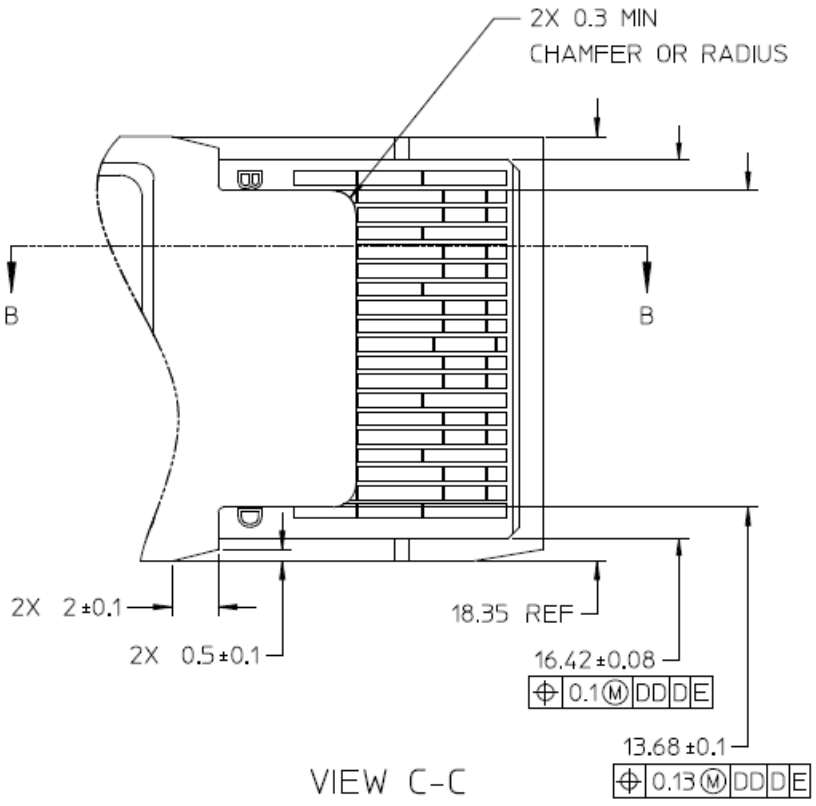
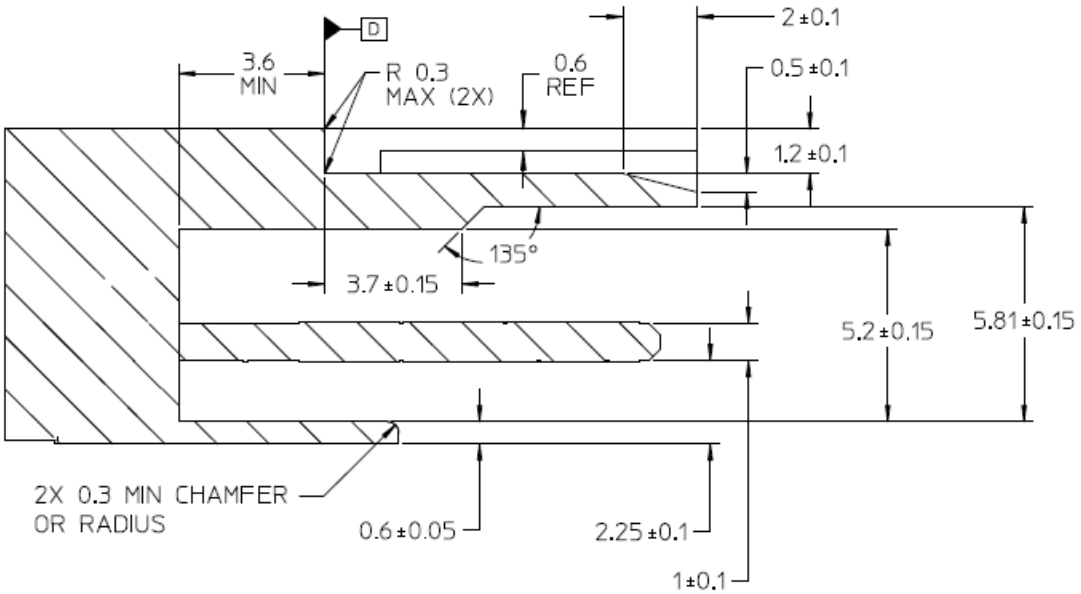


Figure 14: Drawing of module



VIEW C-C



SECTION B-B

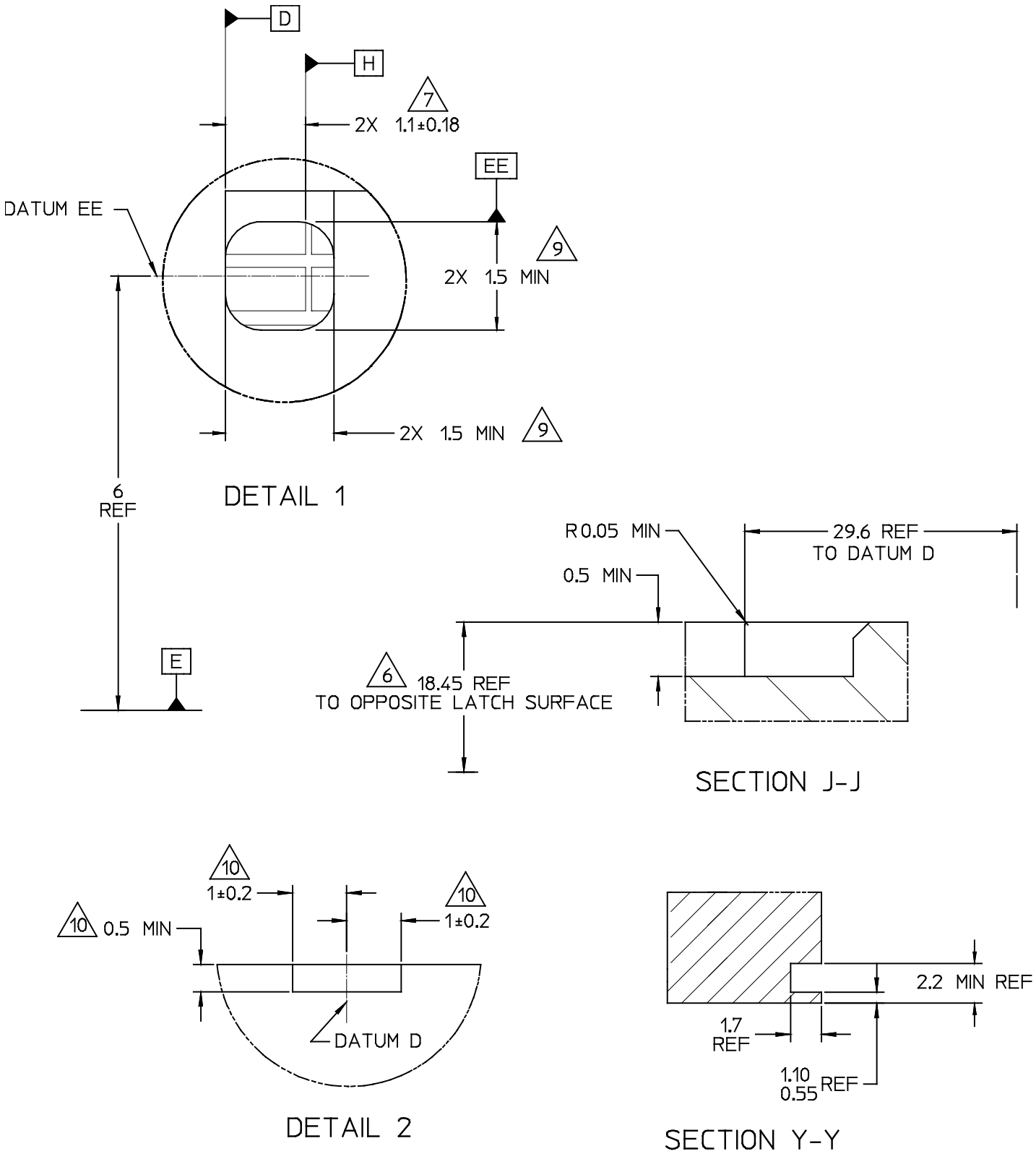


Figure 15: Detailed dimension of module

5.4 Module Flatness and Roughness

Module flatness and roughness are specified to improve module thermal characteristics when used with a riding heat sink. Relaxed specifications are used for lower power modules to reduce cost. The module flatness and roughness specifications apply to the specified heat sink contact area as specified in Figure 14.
Specifications for Module flatness and surface roughness are shown in Table 6 (see Figure 14 note 11).

Table 6- Module flatness specifications

Power Class	Module Flatness (mm)	Surface Roughness (Ra,µm)
1	0.075	1.6
2	0.075	1.6
3	0.075	1.6
4	0.075	1.6
5	0.050	0.8
6	0.050	0.8
7	0.050	0.8
8	0.050	0.8

5.5 Module paddle card dimensions

NOTES APPLY TO MODULE PADDLE CARD :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. NO SOLDER MASK WITHIN 0.05 MM OF ALL DEFINED CONTACT PAD EDGES
4. NO SOLDER MASK BETWEEN END CONTACTS AND THE SIDES OF THE PADDLE CARD

△5 DATUM H IS ESTABLISHED WITH DATUM TARGET POINTS AT THE LEADING EDGE OF THE OUTER MOST SIGNAL CONTACTS PADS TO BE RE-ESTABLISHED ON EACH SIDE

△6 DIMENSION APPLIES FROM THE FIRST SET OF SIGNAL PADS TO THE SECOND SET OF SIGNAL PADS

△7 DIMENSION AND TOLERANCE APPLIES TO ALL GROUND PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

△8 DIMENSION AND TOLERANCE APPLIES TO ALL POWER PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

△9 DIMENSION AND TOLERANCE APPLIES TO ALL SIGNAL PADS ON BOTH TOP AND BOTTOM SIDE OF PADDLE CARD

△10 A ZERO GAP IS ALLOWED FOR A CONTINUOUS PAD OPTION

△11 APPLIES TO ALL SIGNAL PAD TO PAD SPACING

△12 PRE-WIPE PADS (SHADED AREA) ON MODULE CARD HOST SIDE ARE OPTIONAL

△13 PRE-WIPE PADS (UNSHADED AREA) ARE REQUIRED EXCEPT IN CONTINUOUS POWER OR GROUND PAD DESIGNS

△14 PADDLE CARD THICKNESS IS MEASURED OVER PADS VIAS MUST NOT BE PROUD OF THE PAD SURFACE

△15 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND GROUND PADS

△16 MINIMUM DIMENSION REQUIRED FOR MATING SEQUENCE BETWEEN SIGNAL AND POWER PADS

△17 COMPONENT KEEP OUT AREA MEASURED FROM DATUM H

△18 A SINGLE SPLIT IN THE PRE-WIPE SIGNAL PAD IS OPTIONAL, AND IF IMPLEMENTED, THE RESULTING 2 PADS SHALL BE SEPARATED WITH A GAP OF 0.13 ± 0.05

19. CONTACT PAD PLATING
    0.38 MICROMETERS MINIMUM GOLD OVER
    1.27 MICROMETERS MINIMUM NICKEL
    ALTERNATE CONTACT PAD PLATING
    0.05 MICROMETERS MINIMUM GOLD OVER
    0.30 MICROMETERS MINIMUM PALLADIUM OVER
    1.27 MICROMETERS MINIMUM NICKEL

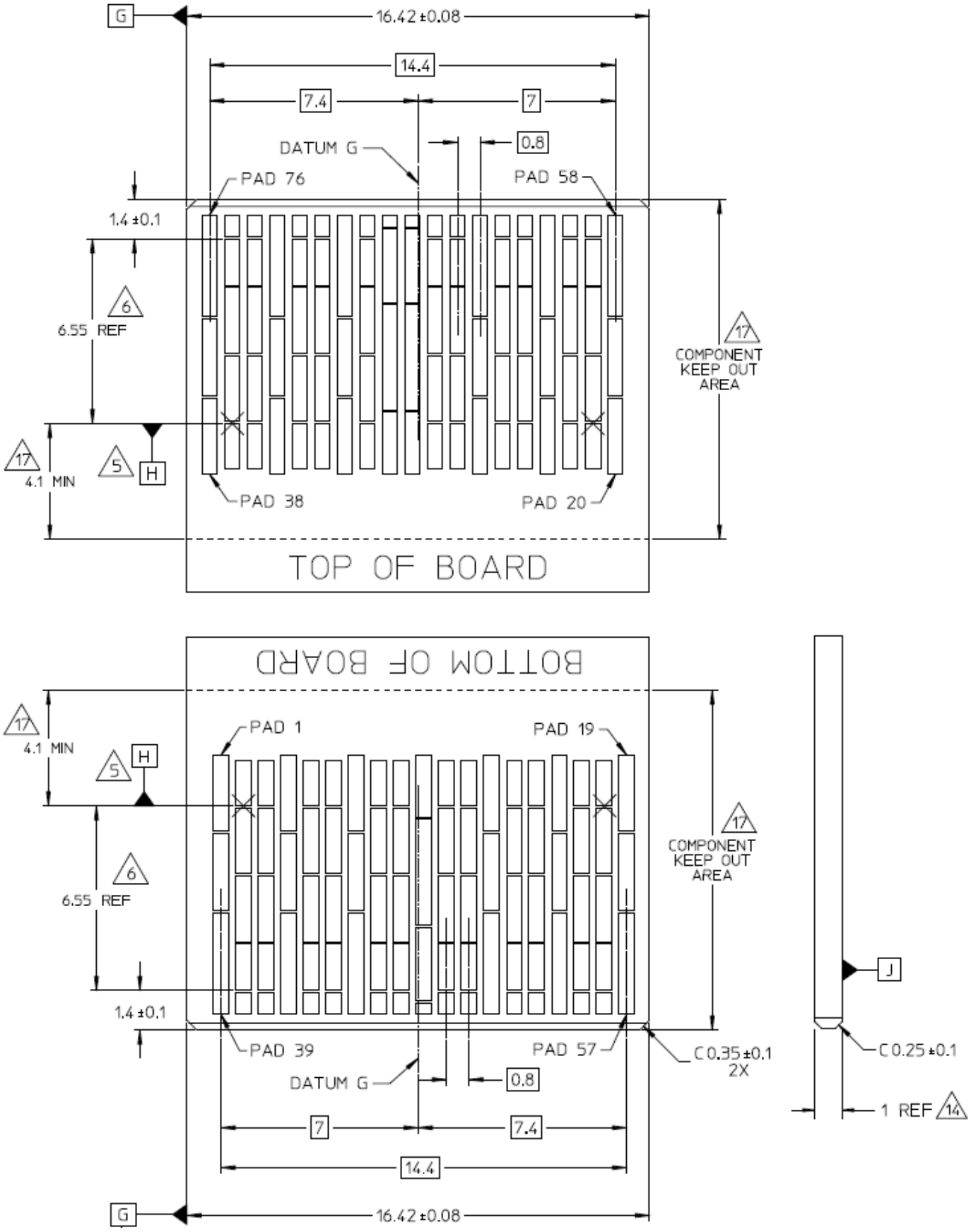


Figure 16: Module paddle card dimensions

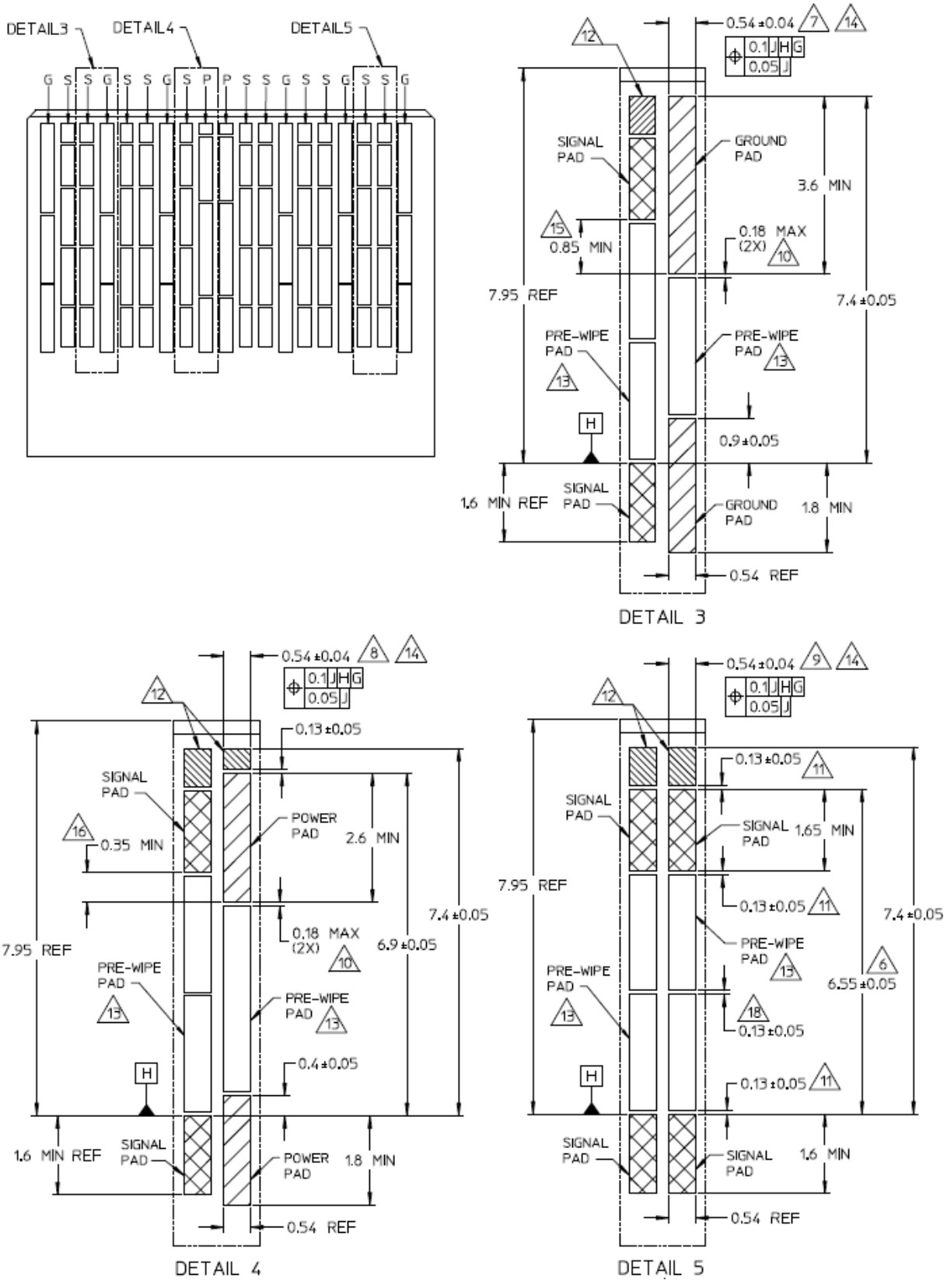


Figure 17: Module pad dimensions

5.6 Module Extraction and Retention Forces

The requirements for insertion forces, extraction forces and retention forces are specified in Table 7. The QSFP-DD cage and module are designed to ensure that excessive force applied to a cable does not damage the QSFP-DD cage or host connector. If any part is damaged by excessive force, it should be the cable or media module and not the cage or host connector which is part of the host system. The contact pad plating shall meet the requirements of Section 5.5.

Table 7- Insertion, Extraction and Retention Forces

Measurement	Min	Max	Units	Comments
QSFP module insertion	0	40	N	
QSFP-DD module insertion	0	90	N	
QSFP module extraction	0	30	N	
QSFP-DD module extraction	0	30	N	
QSFP module retention	90	N/A	N	No damage to module below 90N with latch engaged
QSFP-DD module retention	90	N/A	N	No damage to module below 90N with latch engaged
Cage retention (Latch strength)	180	N/A	N	No damage to latch below 180N
Cage retention in Host Board	114	N/A	N	Force to be applied in a vertical direction, no damage to cage
Insertion / removal cycles, connector / cage	100	N/A	Cycles	Number of cycles for the connector and cage with multiple modules.
Insertion / removal cycles, QSFP-DD module	50	N/A	Cycles	Number of cycles for an individual module.
Note: Insertion, Extraction and Retention forces are specified without a riding heat sink.				

5.7 2x1 Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The integrated connector in a 2x1 stacked cage is shown in Figure 18 with detailed drawings in Figure 19, Figure 20 and Figure 21. Recommendations for the 2x1 stacked cage bezel opening are shown in Figure 22.

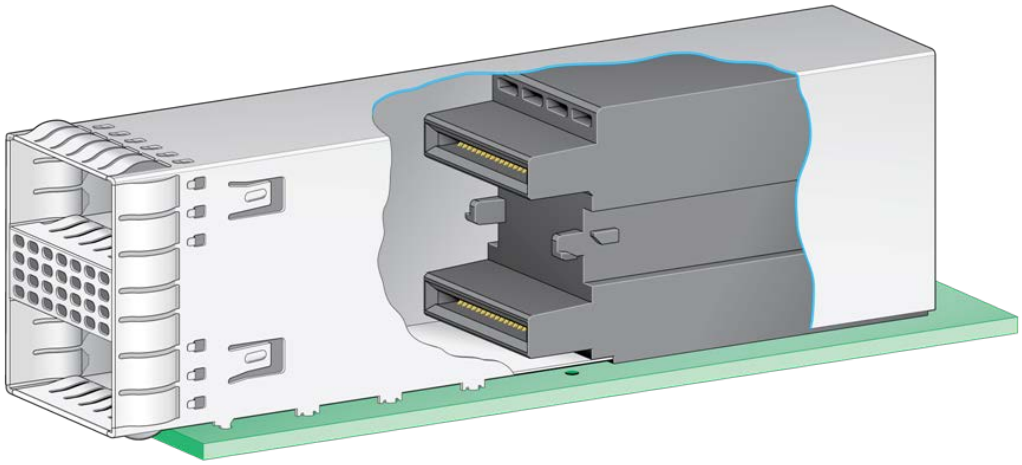


Figure 18: Integrated connector in 2x1 stacked cage

NOTES APPLY TO 2X1 STACKED CAGE :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

3. DIMENSIONS FROM INSIDE SURFACES OF GASKETS WHEN FULLY DEPRESSED

4. CONNECTOR REMOVED FOR DRAWING CLARITY.

5. APPLIES TO ALL SPRING FINGERS ON ALL SIDES.

6. EXTERNAL CAGE DIMENSIONS. DOES NOT INCLUDE FOLDING TABS.

7. LENGTH OF CAGE AND SIGNAL TAILS.

8. PRESS FIT CAGE PINS APPLY TO RIGHT SIDE OF CAGE.

9. PRESS FIT CAGE PINS APPLY TO LEFT SIDE TO CAGE.

10. PRESS FIT PIN OFFSET BETWEEN RIGHT AND LEFT SIDE OF CAGE.

11. DIMENSIONS INCLUDES BACKCOVER.

12. SIZE AND POSITION OF CAGE AND CONNECTOR PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT

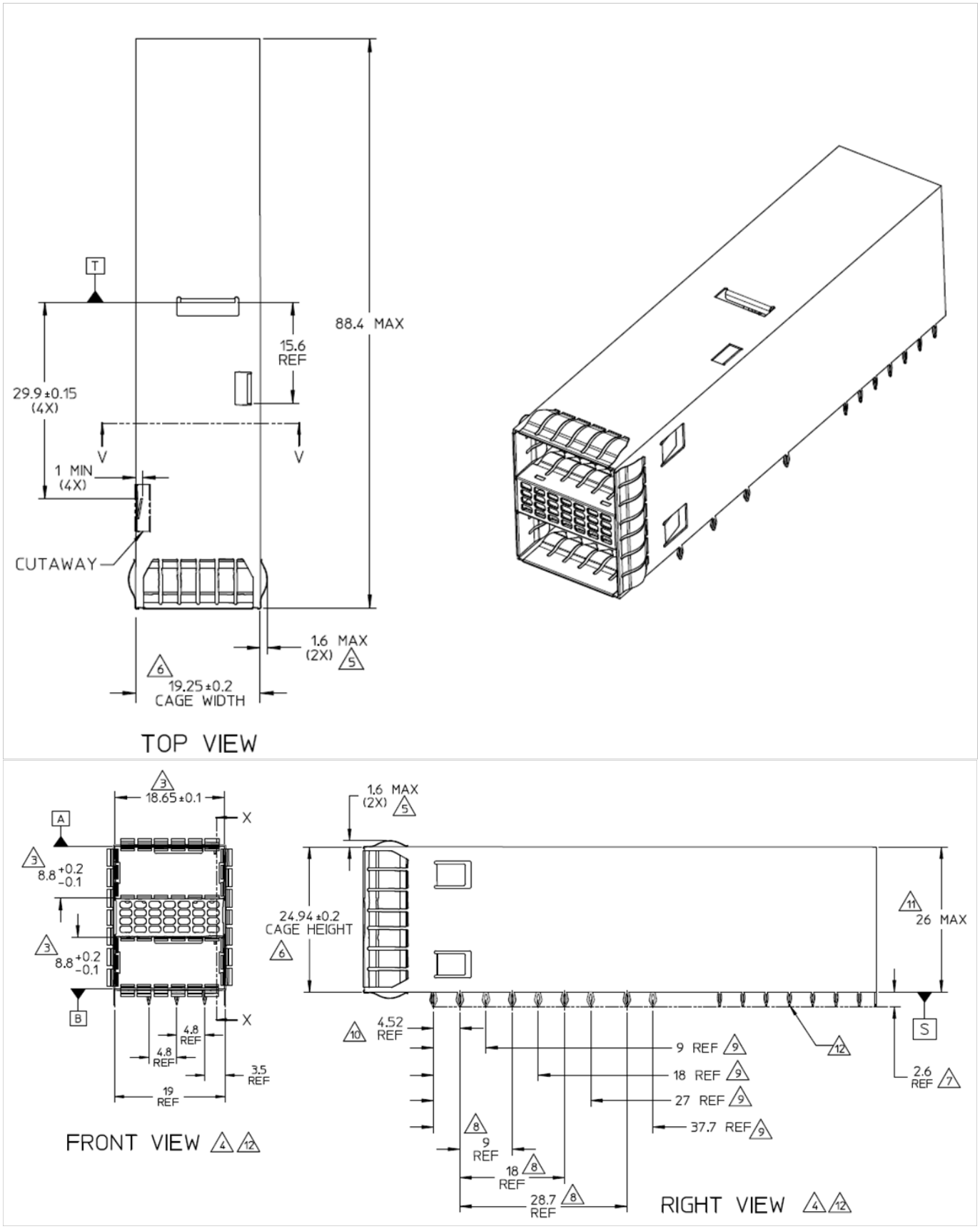
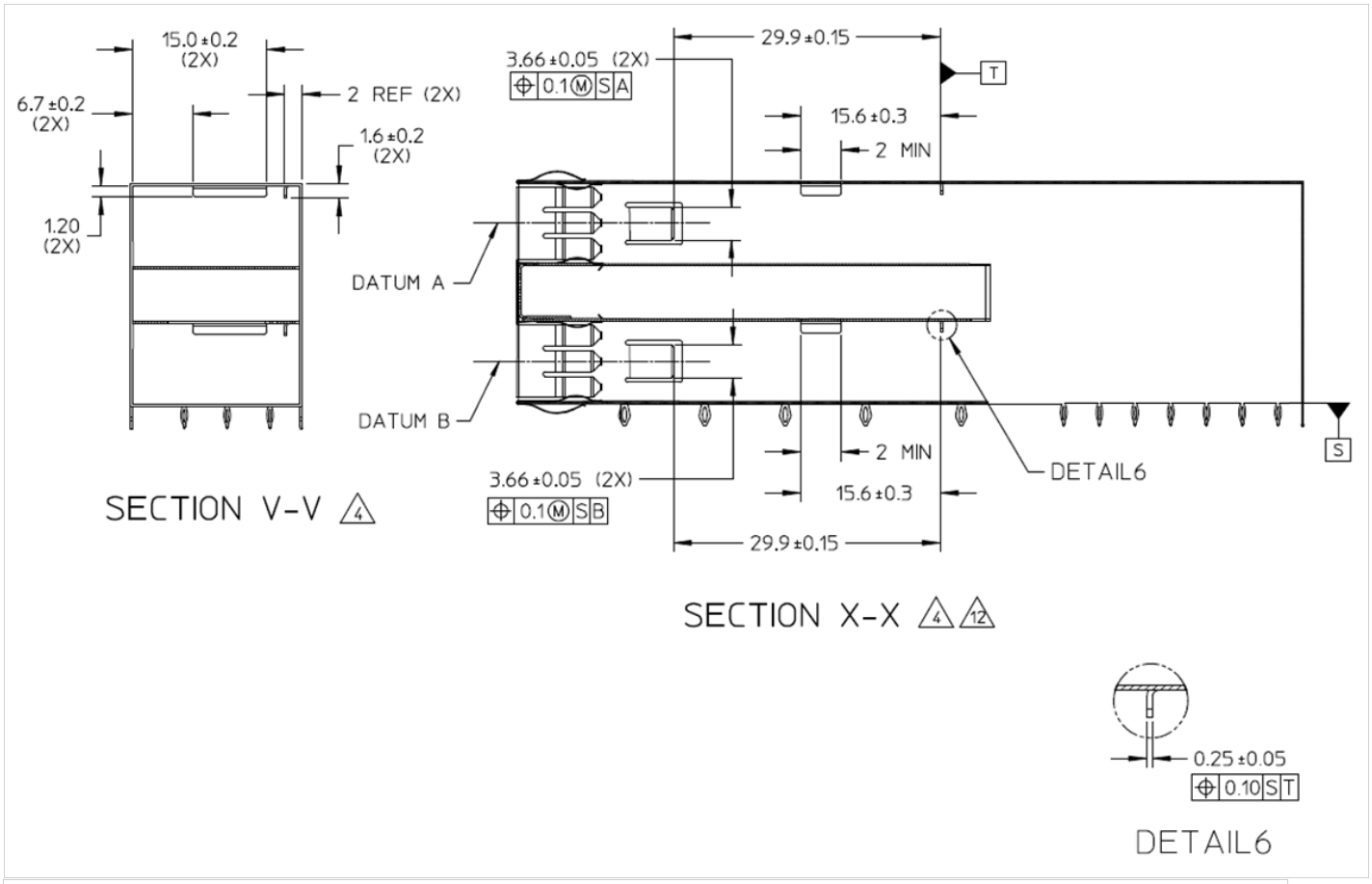


Figure 19: 2x1 stacked cage



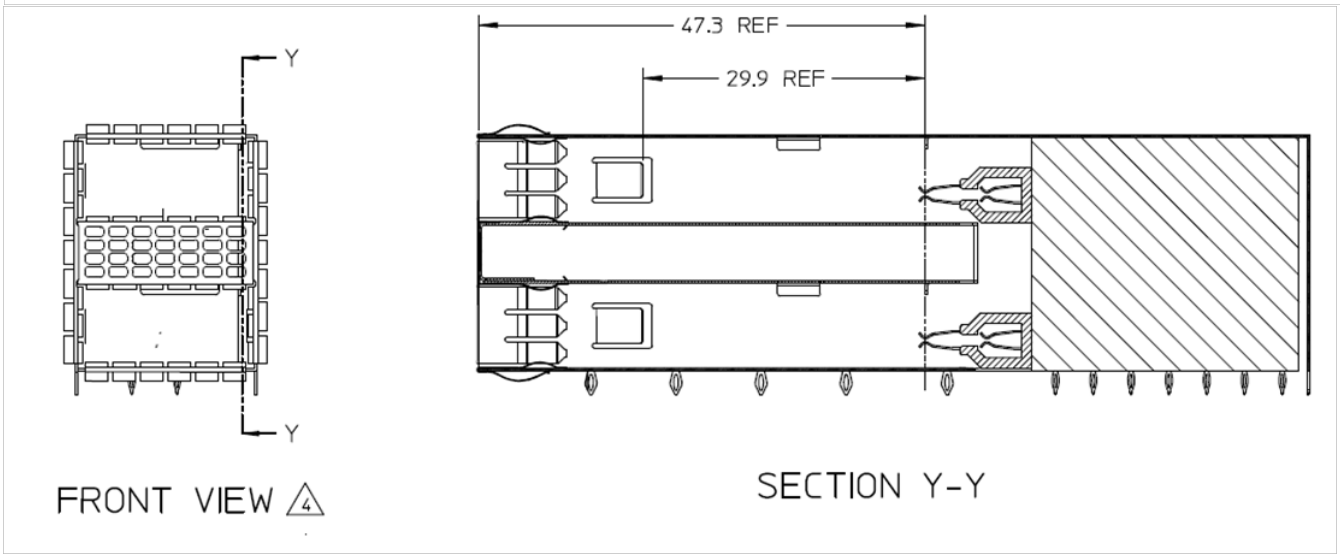


Figure 20: 2x1 stacked cage dimensions

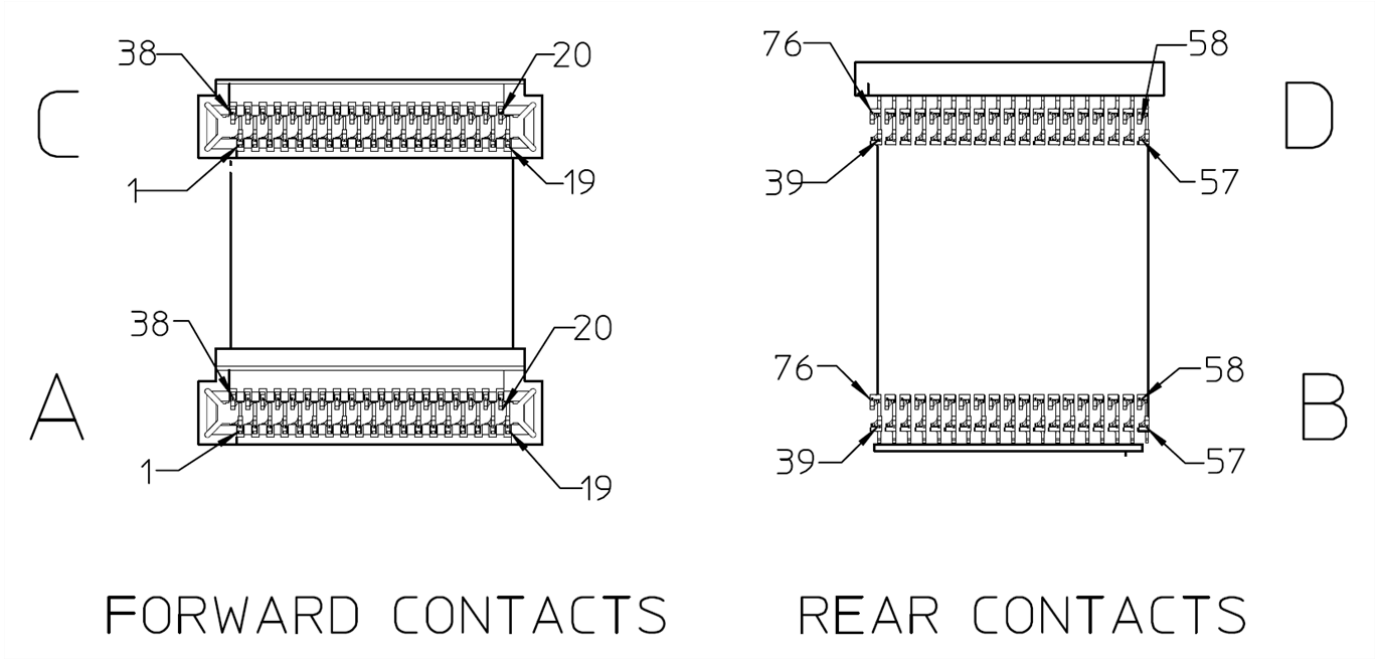


Figure 21: Connector pins in 2x1 stacked cage as viewed from the front

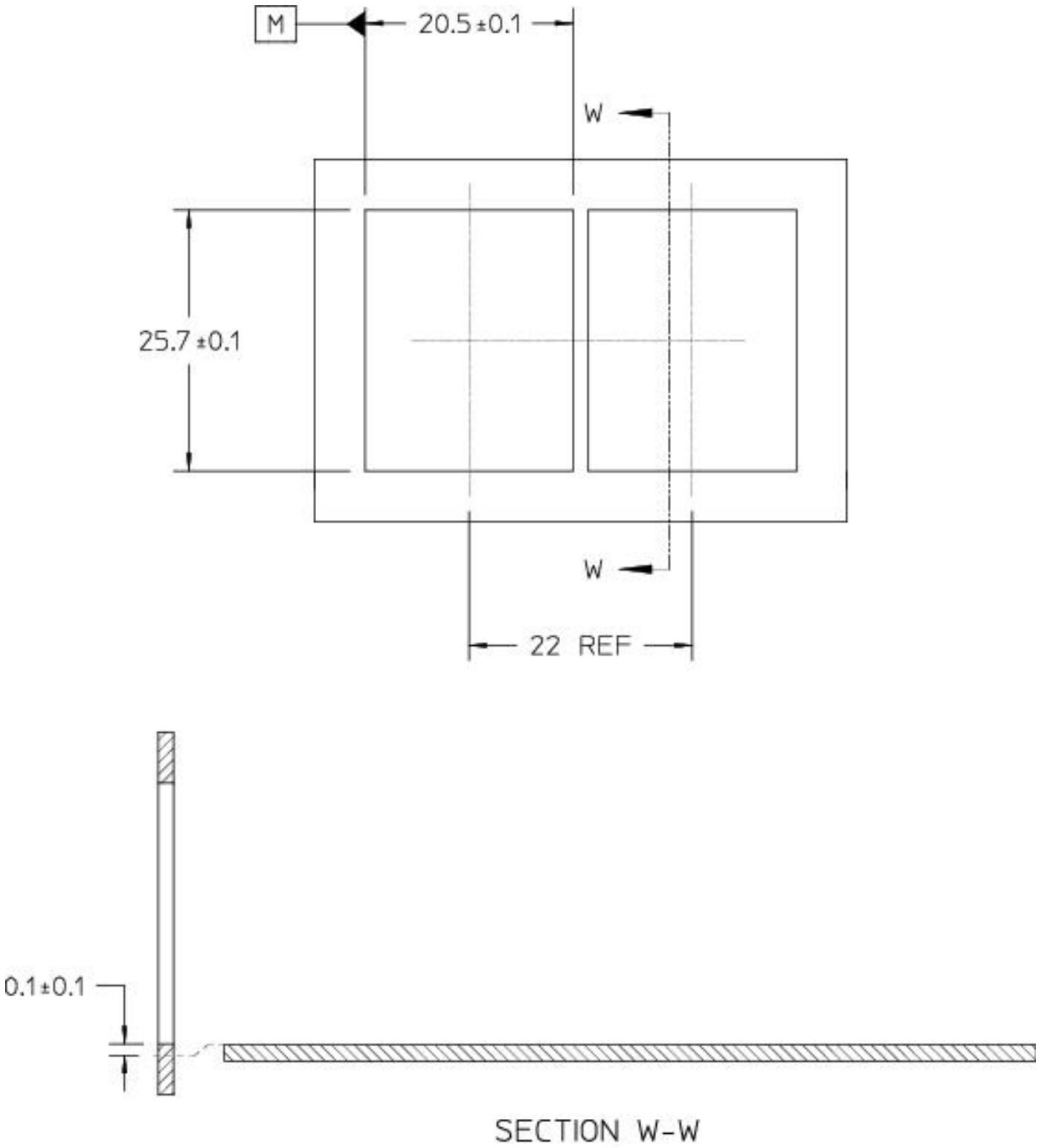


Figure 22: 2x1 Bezel Opening

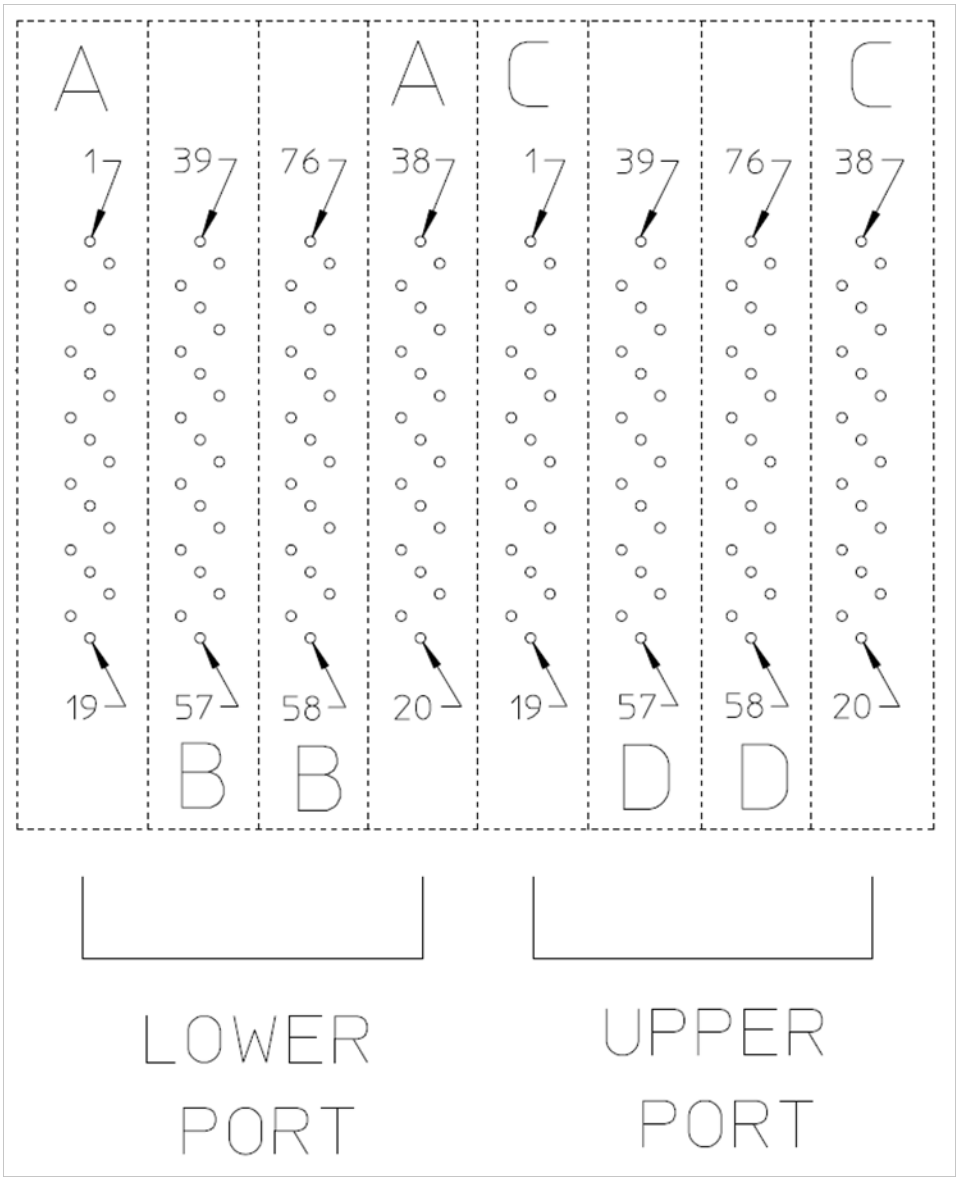


Figure 23: 2X1 host board connector contacts

5.7.1 2x1 Connector and Cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD 2x1 Connector and Cage System is shown in Figure 23 and Figure 24. Location of the pattern on the host board is application specific.

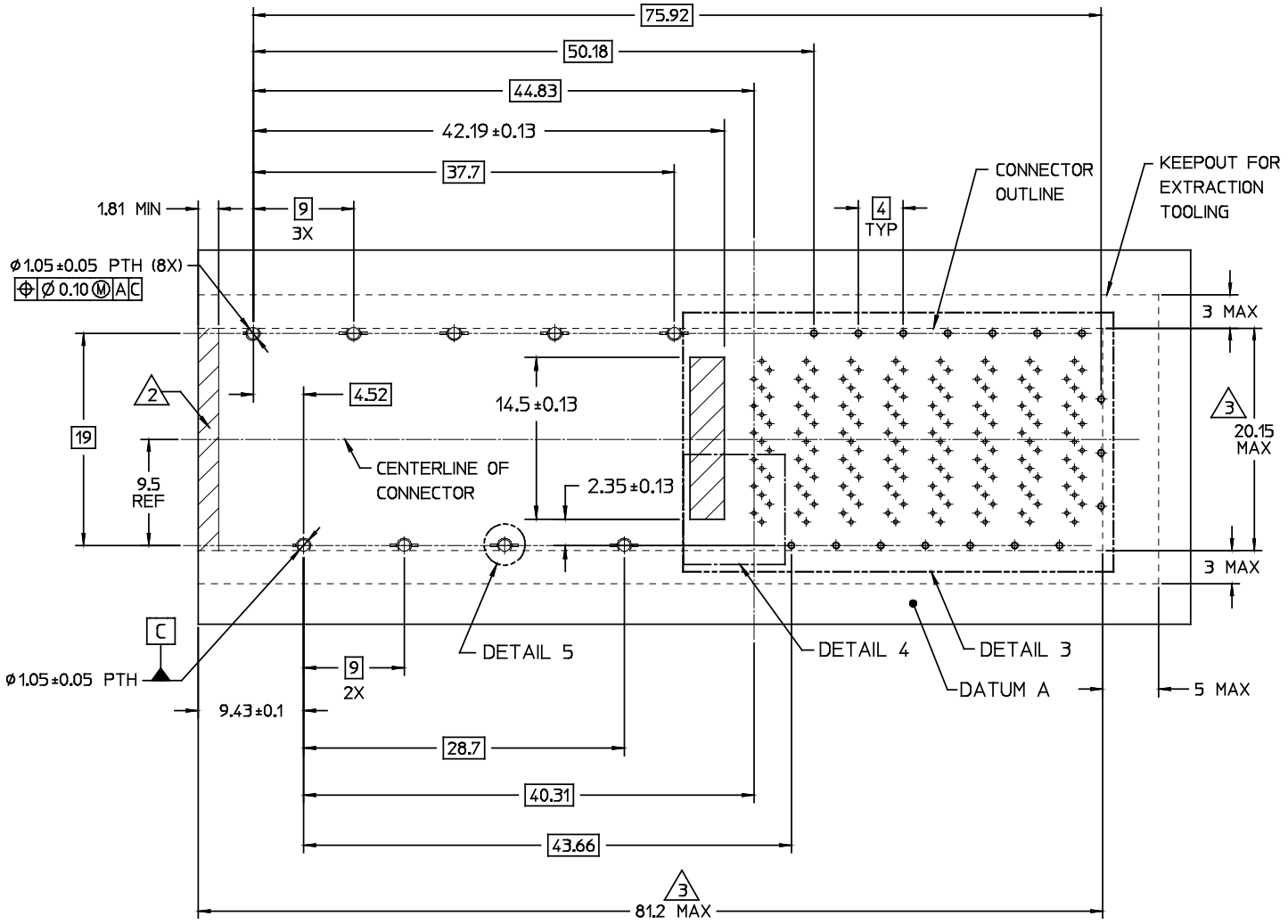
To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

NOTES APPLY TO HOST PCB :

1. THE ENTIRE AREA UNDER THE CONNECTOR (OUTSIDE DASHED LINES) IS TO BE CONSIDERED A KEEP OUT AREA FOR COMPONENTS

2. HATCHED AREA REPRESENT ZONES ON THE PCB THAT COME IN CONTACT WITH OR BE IN CLOSE PROXIMITY TO THE PLASTIC HOUSING OR THE CONNECTOR CAGE. INDICATED AREAS TO BE CONSIDERED TRACE FREE.

3. DIMENSION APPLIES TO CONNECTOR OUTLINE



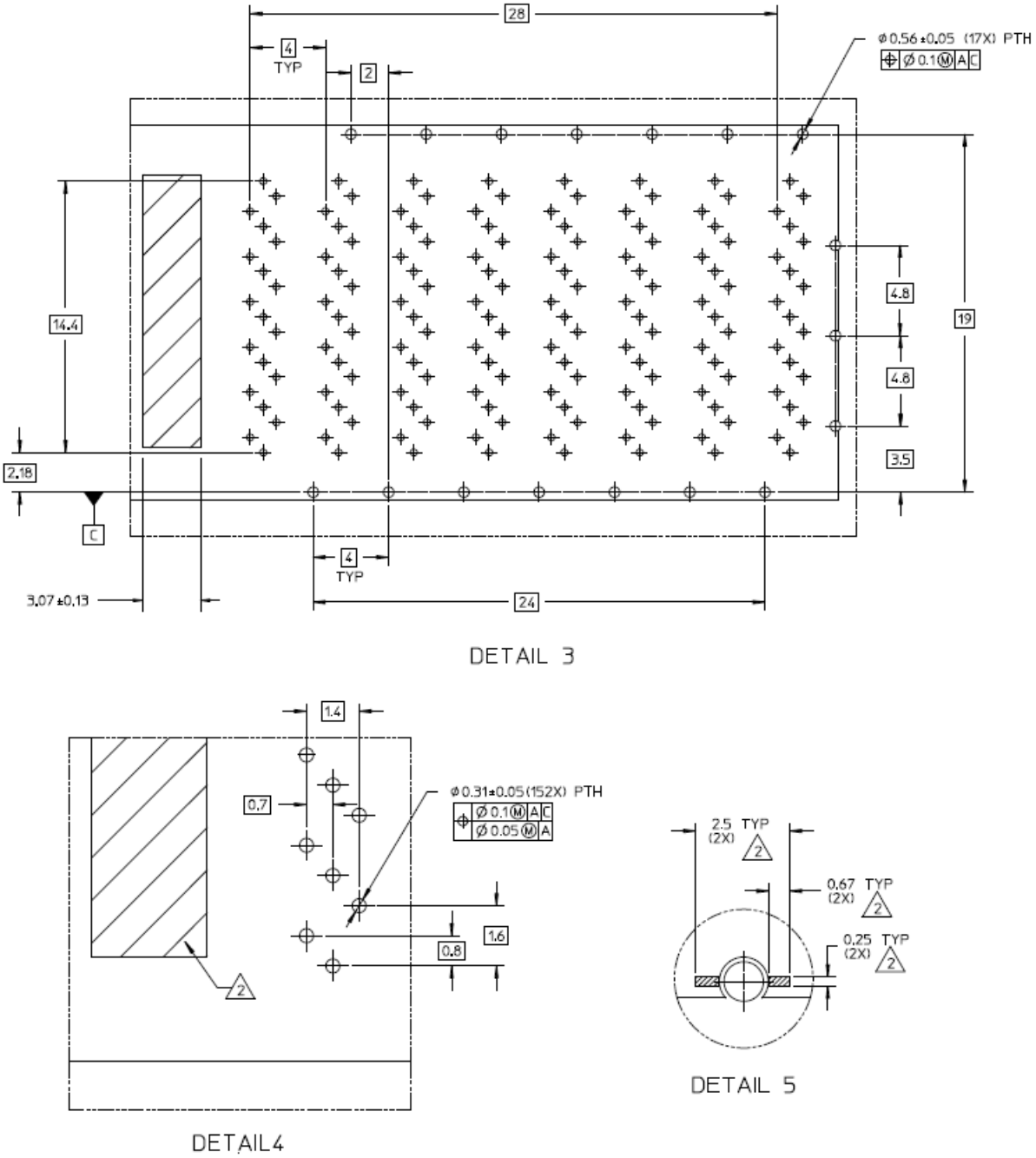


Figure 24: 2X1 Host PCB Mechanical Layout

5.8 Surface Mount Electrical Connector Mechanical

The QSFP-DD Connector is a 76-contact, right angle connector. The SMT connector in a 1xn cage is shown in Figure 25 with detailed drawings in Figure 26 and Figure 27. Recommendations for the SMT cage bezel opening are shown in Figure 28.

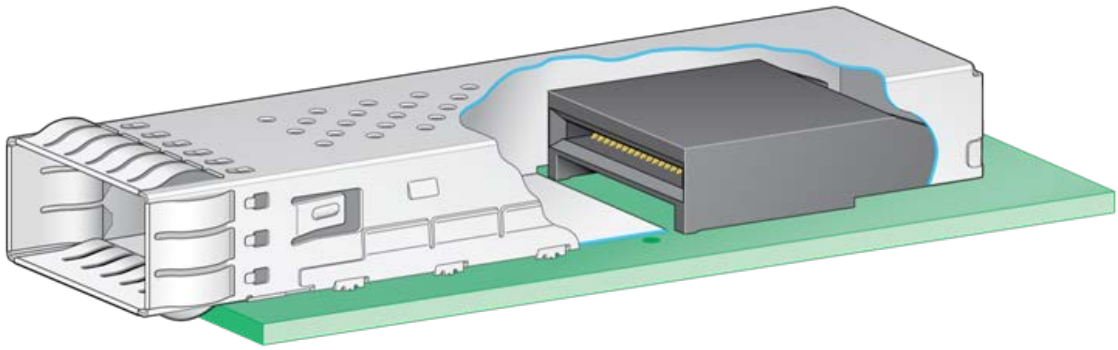


Figure 25: SMT connector in 1xn cage

NOTES APPLY TO SMT 1 X N CAGE DRAWINGS :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2009

2. ALL DIMENSIONS ARE IN MILLIMETERS.

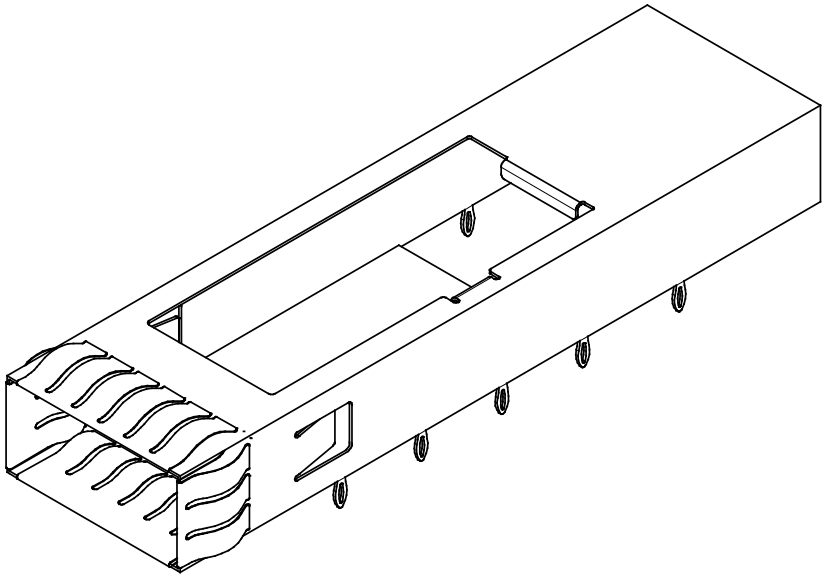
△3 DIMENSIONS FROM INSIDE SURFACES OF GASKETS WHEN FULLY DEPRESSED.

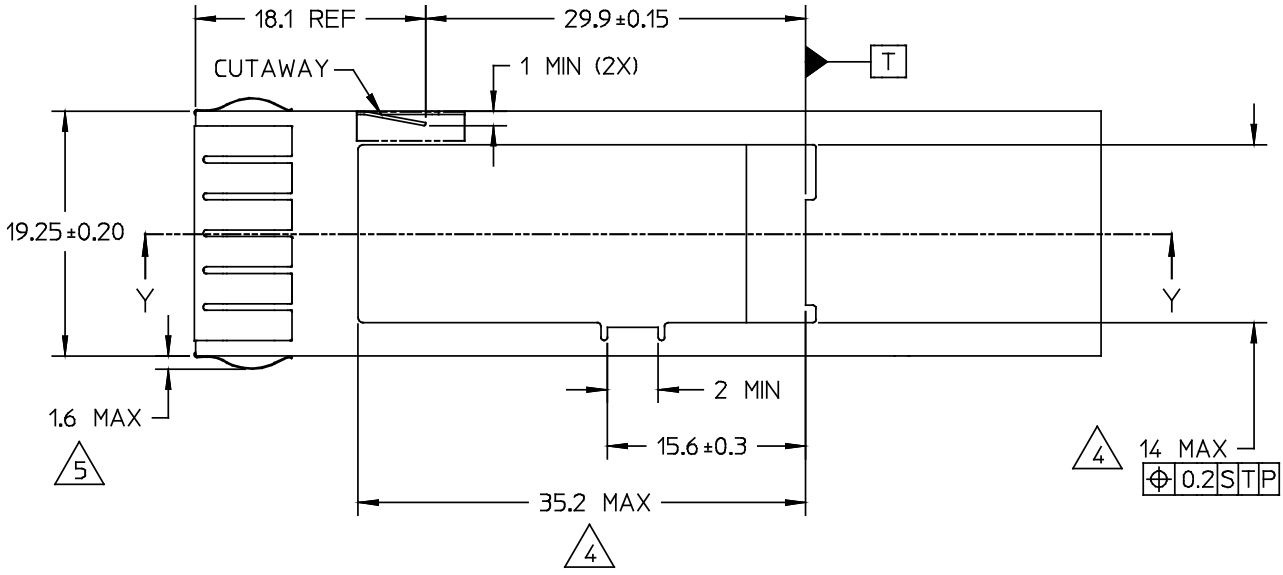
△4 CAVITY FOR HEAT SINK IS OPTIONAL.

△5 APPLIES TO ALL SPRING FINGERS ON ALL SIDES.

△6 DATUM S IS DEFINED BY SEATING PLANE ON HOST BOARD.

△7 SIZE AND POSITION OF CAGE PRESS FIT PINS SHALL BE DEFINED BY EACH SUPPLIER BASED UPON THE PCB FOOTPRINT LAYOUT.




18.1 REF
29.9±0.15
CUTAWAY
1 MIN (2X)
T
19.25±0.20
Y
Y
1.6 MAX
5
2 MIN
15.6±0.3
35.2 MAX
4
4
14 MAX
0.2 S T P

TOP VIEW

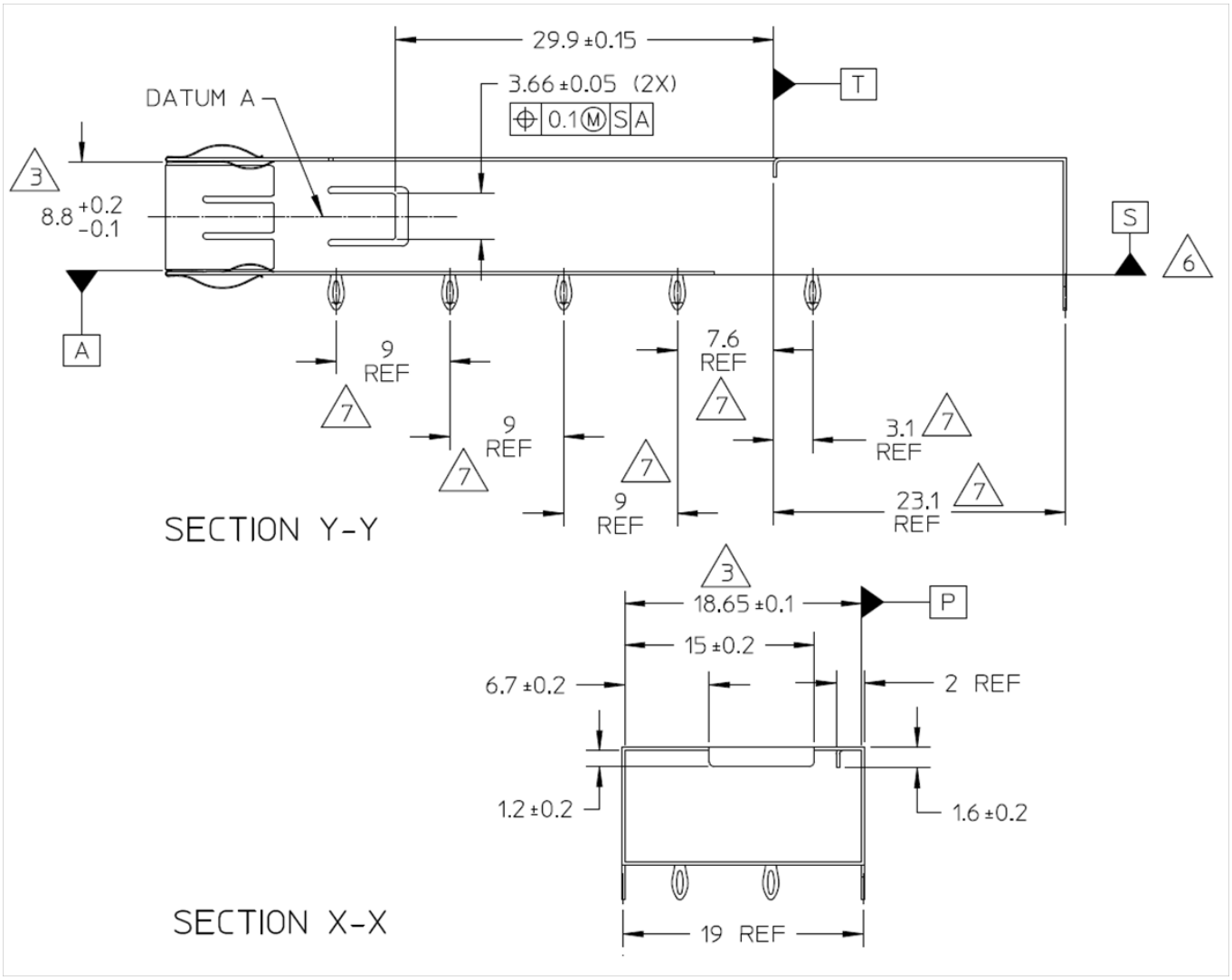
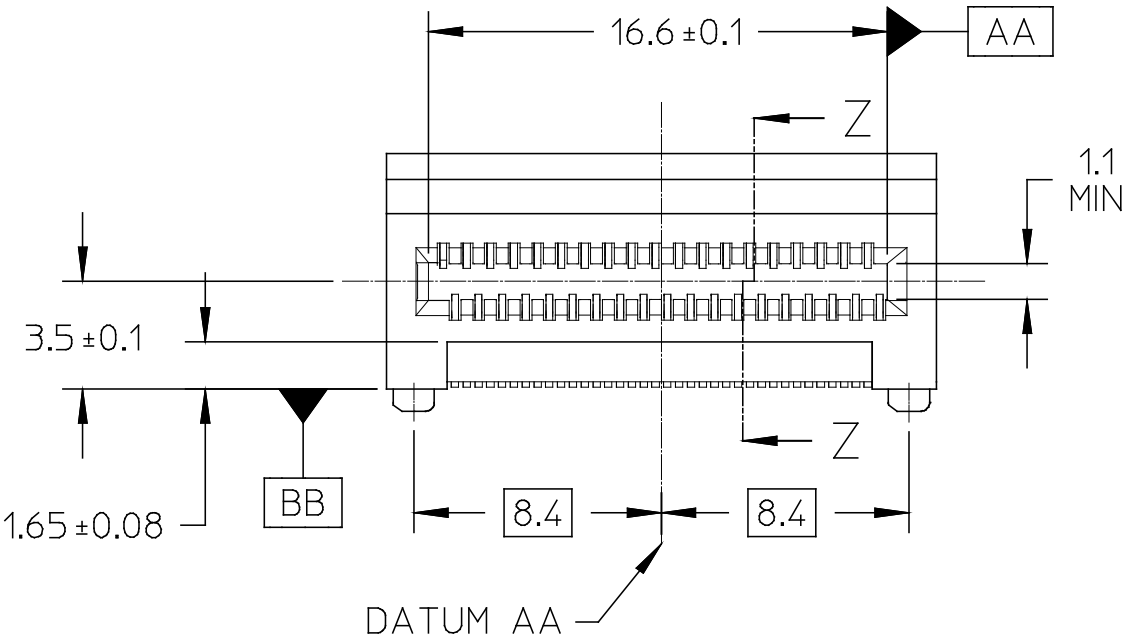
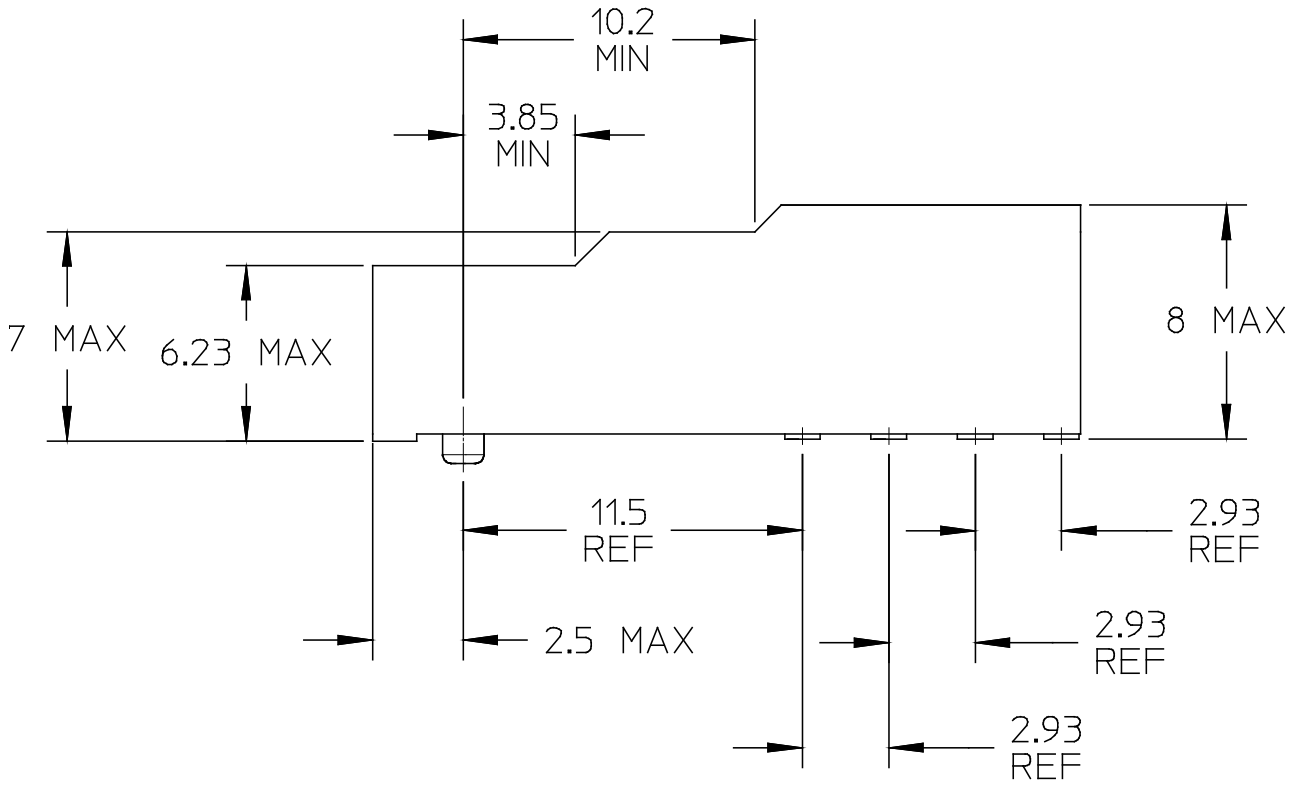


Figure 26: SMT 1x1 Cage Design



FRONT VIEW



SIDE VIEW

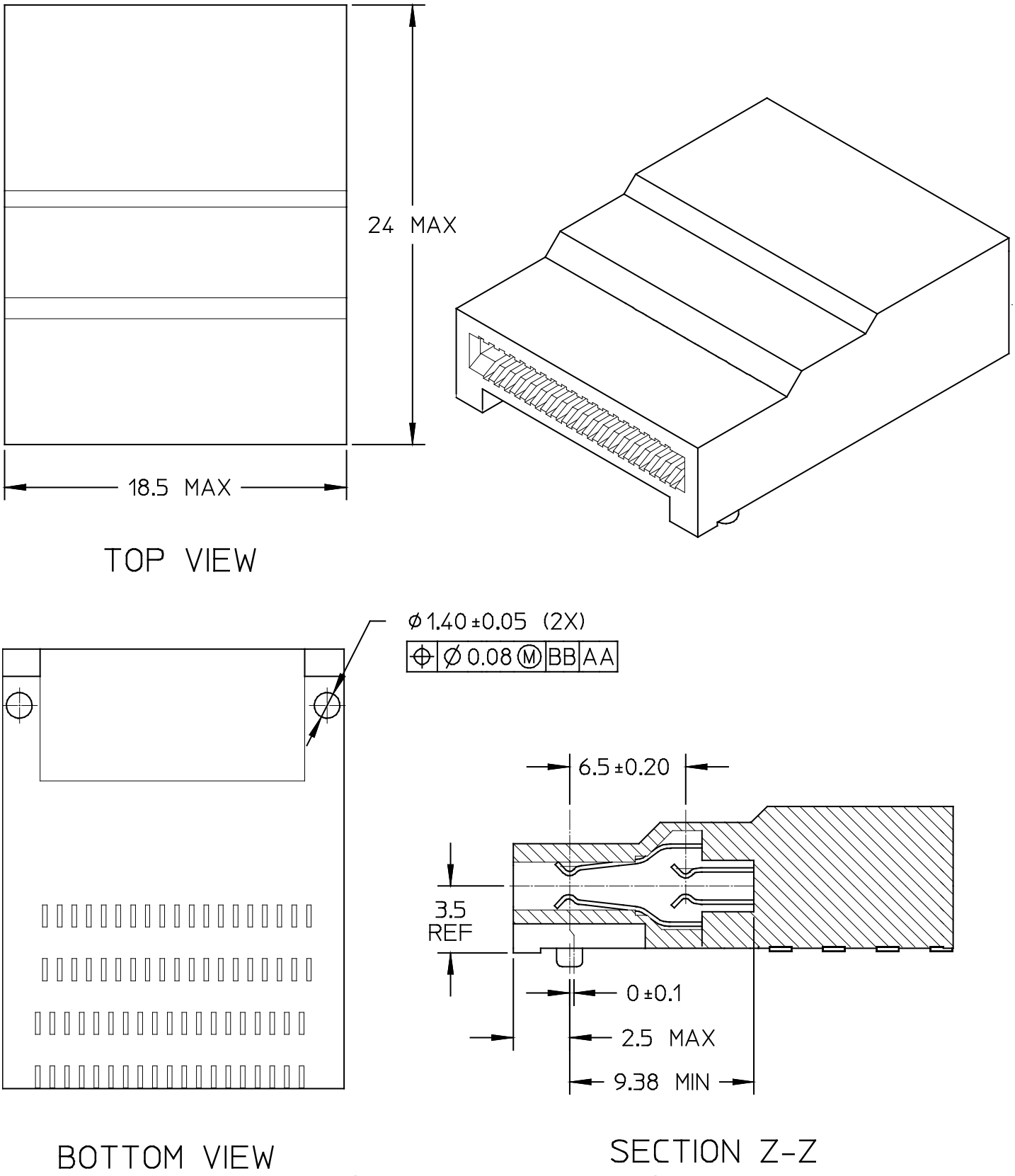


Figure 27: SMT 1x1 Connector Design

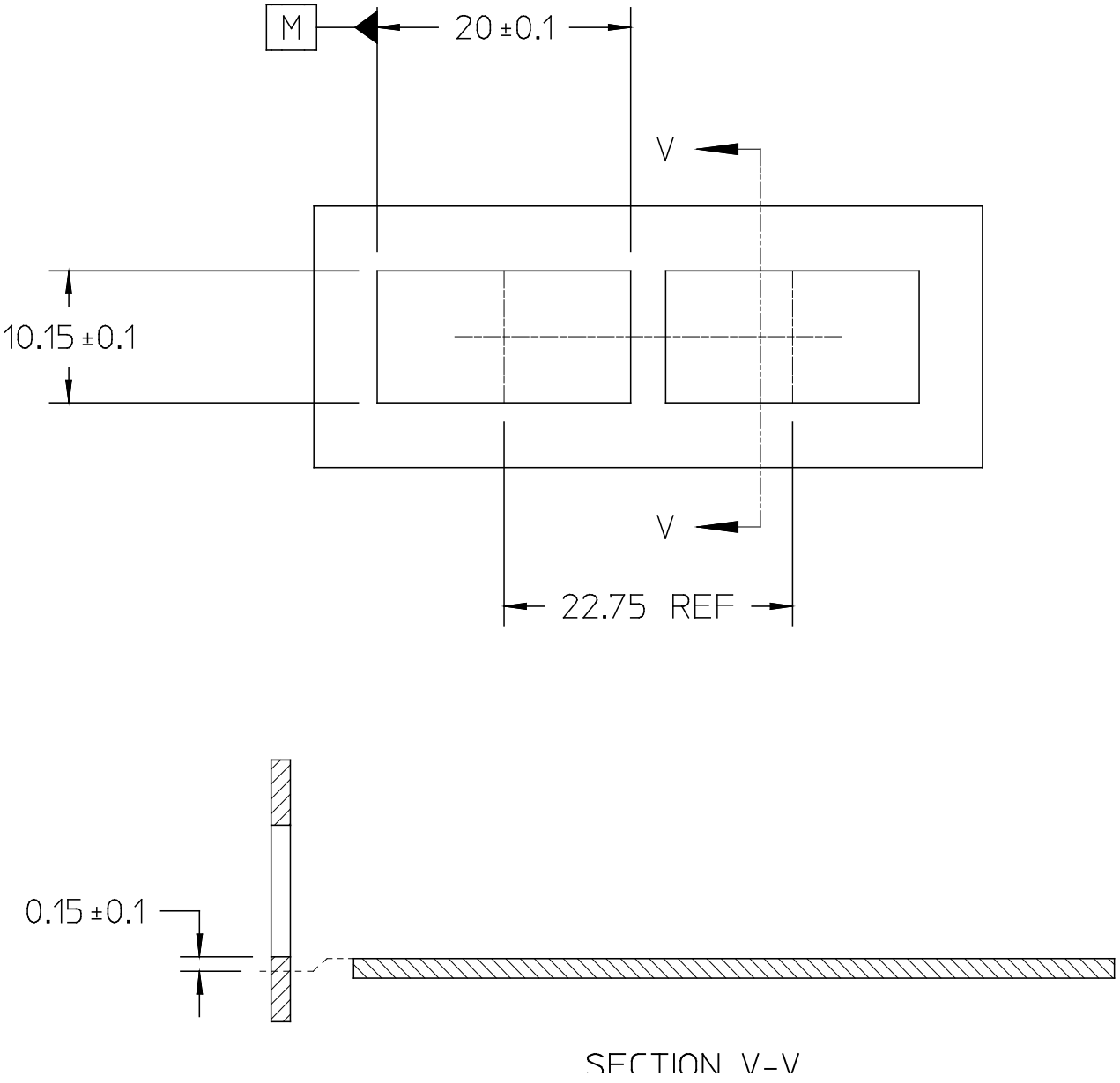


Figure 28: SMT 1xn bezel opening

5.8.1 Surface mount connector and cage host PCB layout

A typical host board mechanical layout for attaching the QSFP-DD surface mount Connector and Cage System is shown in Figure 29 and Figure 30. Location of the pattern on the host board is application specific.

To achieve 25-50 Gbps performance pad dimensions and associated tolerances must be adhered to and attention paid to the host board layout.

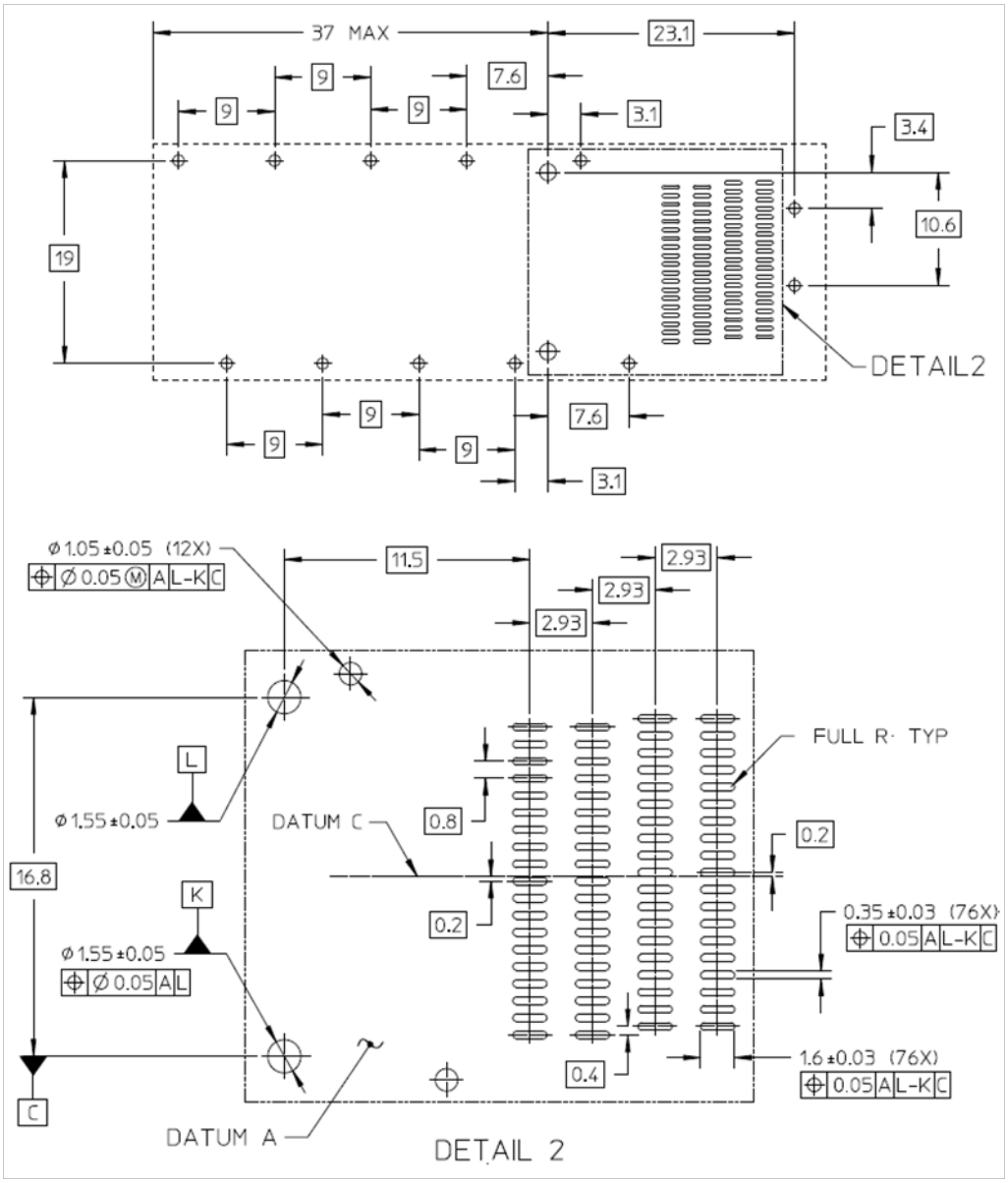


Figure 29: SMT Host PCB Mechanical Layout

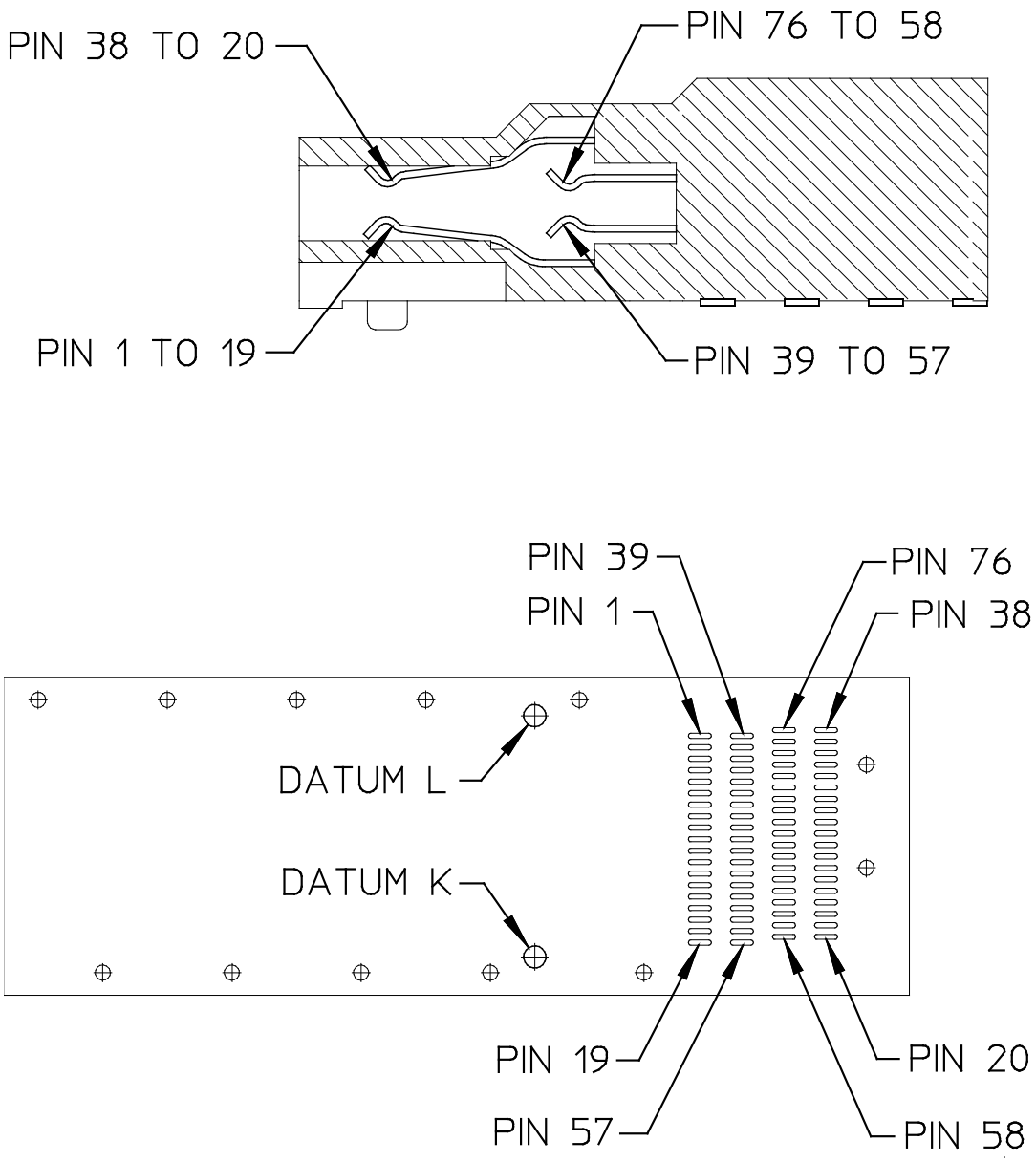


Figure 30: SMT Connector and Host PCB Pin Numbers

5.9 Module Color Coding and Labeling

An exposed feature of the QSFP-DD module (a feature or surface extending outside of the bezel) shall be color coded as follows:

Beige for 850nm
Blue for 1310nm
White for 1550nm

Each QSFP-DD module shall be clearly labeled. The complete labeling need not be visible when the QSFP-DD module is installed and the bottom of the device is the recommended location for the label. Labeling shall include:

Appropriate manufacturing and part number identification
Appropriate regulatory compliance labeling
A manufacturing traceability code

The label should also include clear specification of the external port characteristics such as:

Optical wavelength
Required fiber characteristics
Operating data rate
Interface standards supported
Link length supported

The labeling shall not interfere with the mechanical, thermal or EMI features.

5.10 Optical Interface

The QSFP-DD optical interface port shall be either a male MPO receptacle (see Figure 32, Figure 33 and Figure 34), a dual LC (see Figure 35) or a CS connector (see Figure 37). The recommended location and numbering of the optical ports for each of the Media Dependent Interfaces is shown in Figure 31.

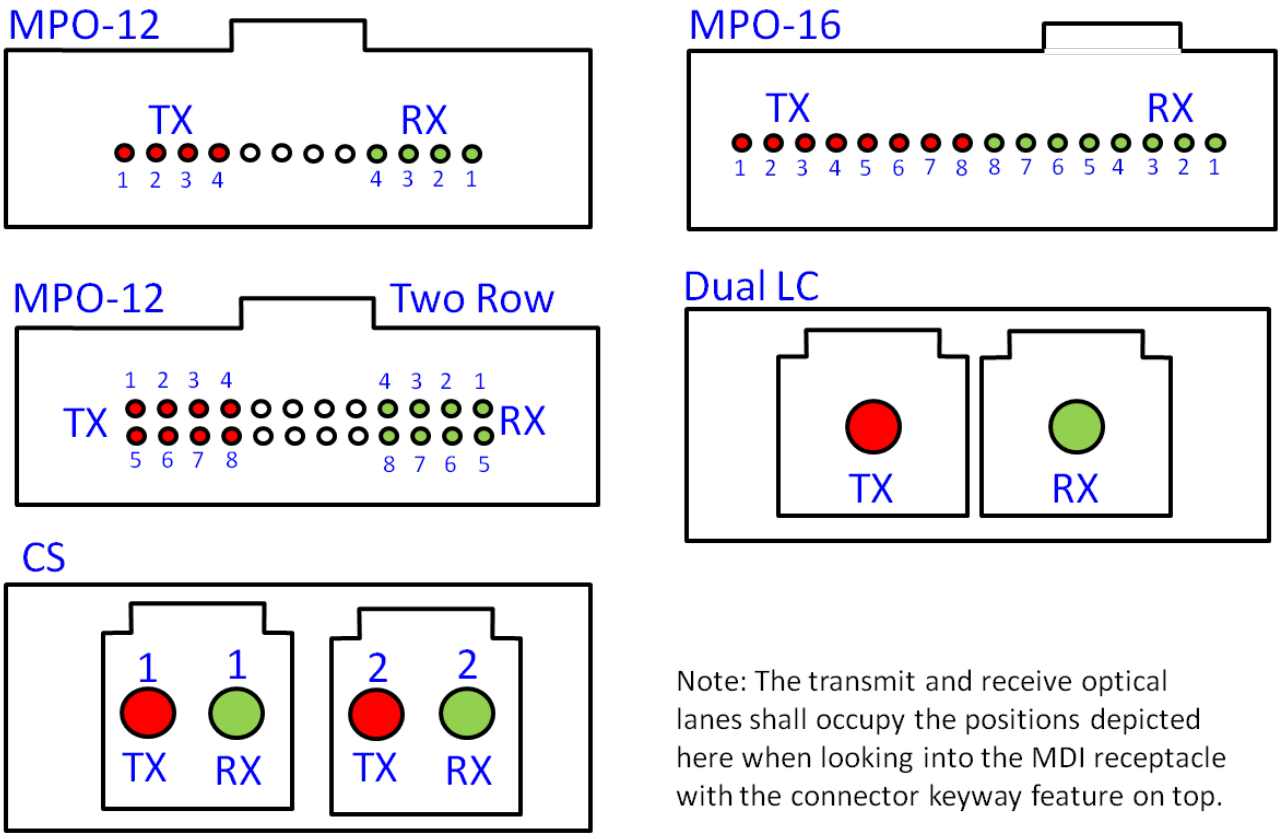


Figure 31: Optical Media Dependent Interface port assignments

5.10.1 MPO Optical Cable connections

The optical plug and receptacle for the MPO-12 connector is specified in TIA-604-5 and shown in Figure 32 (MPO-12 Single Row)and Figure 34 (MPO-12 Two Row). The optical plug and receptacle for the MPO-16 connector is specified in TIA-604-18 and shown in Figure 33 (MPO-16 Single Row). Note: Two alignment pins are present in each receptacle.

Aligned keys are used to ensure alignment between the modules and the patchcords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top.

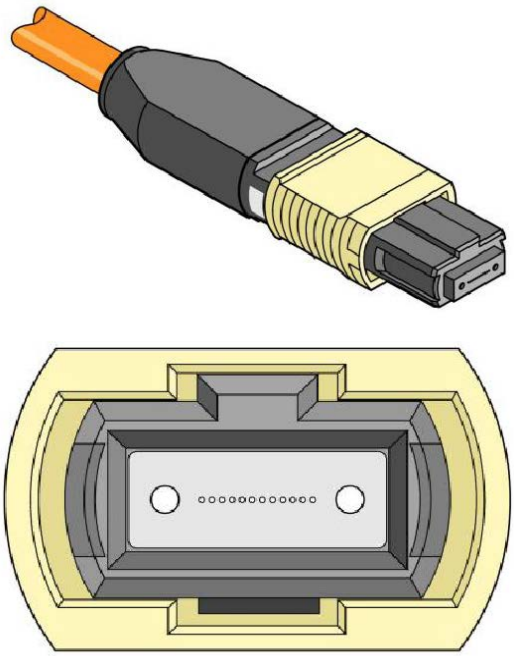


Figure 32: MPO-12 Single Row optical patch cord and module receptacle

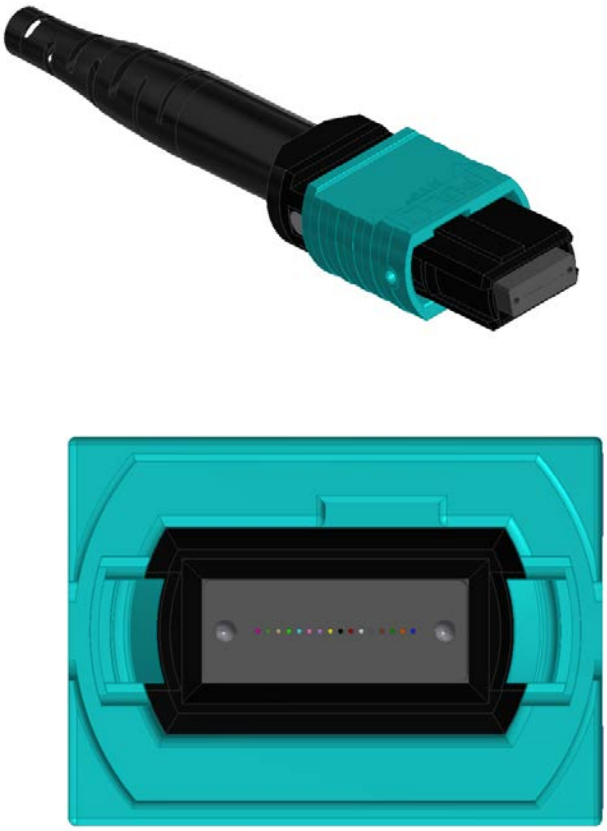


Figure 33: MPO-16 Single Row optical patchcord and module receptacle

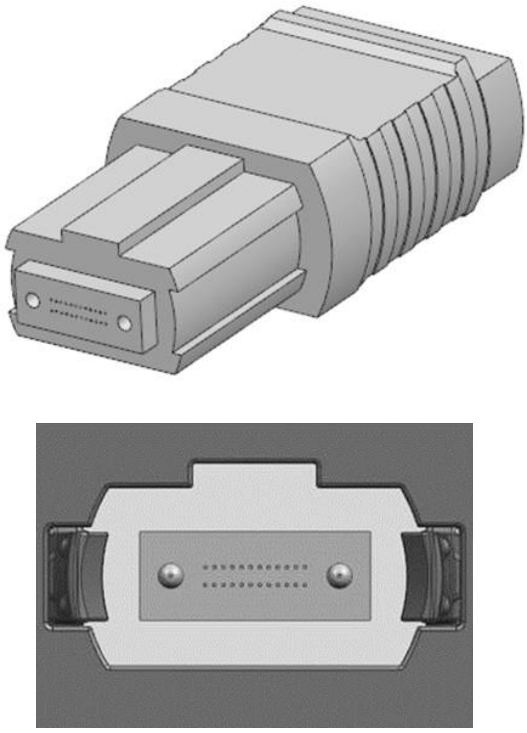


Figure 34: MPO-12 Two Row optical patchcord and module receptacle

5.10.2 Dual LC Optical Cable connection

The Dual LC optical patchcord and module receptacle is specified in TIA-604-10 and shown in Figure 35.

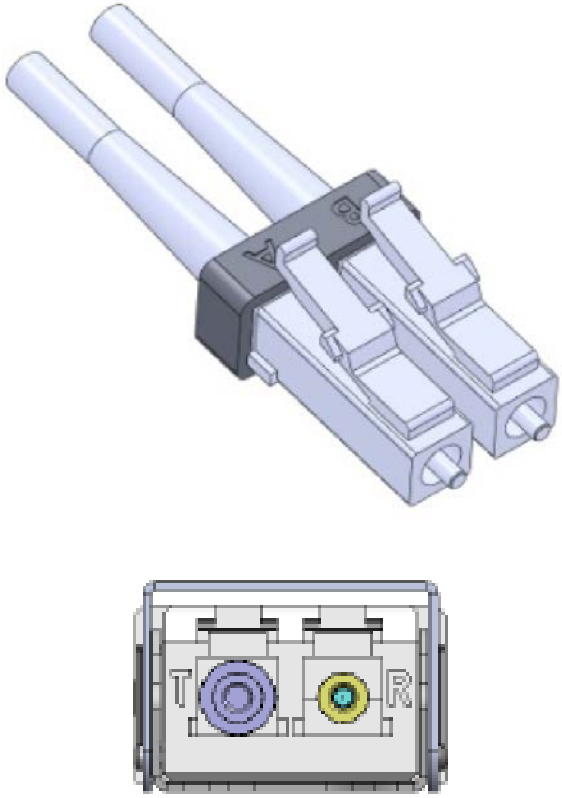


Figure 35: Dual LC optical patchcord and module receptacle

5.10.3 Dual CS Optical Cable connection

The Dual CS optical receptacle for a QSFP-DD module is specified in CS-01242017 (see 2.1 Industry Documents) and shown in Figure 36.

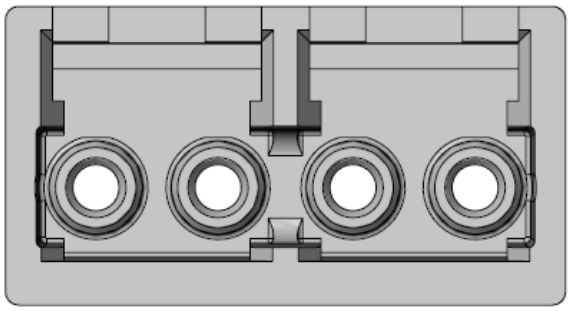


Figure 36: Dual CS connector module receptacle (in support of breakout applications)

5.10.4 Electrical data input/output to optical port mapping

Table 8 defines the mapping of electrical TX data inputs to optical ports. The mapping of the RX optical ports to electrical RX outputs is symmetric. Note that there is no defined mapping of electrical input/output to optical wavelengths for WDM applications.

Table 8- Electrical data input to Optical Port Mapping

Electrical Data Input Reference	Optical Port Type (see Figure 31)			
	LC	CS	MPO-12	MPO-12 (double row) MPO-16
	1 TX fiber[1]	2 Tx fibers[1]	4 Tx fibers[1]	8 Tx fibers[1]
Tx1	TX-1	TX-1	TX-1	TX-1
Tx2				TX-2
Tx3			TX-2	TX-3
Tx4				TX-4
Tx5		TX-2	TX-3	TX-5
Tx6				TX-6
Tx7			TX-4	TX-7
Tx8				TX-8
Note 1: Tx-n, where n is the optical port number as defined in Figure 31				

6 Environmental and Thermal

6.1 Thermal Requirements

The QSFP-DD module shall operate within one or more of the case temperatures ranges defined in Table 9. The temperature ranges are applicable between 60m below sea level and 1800m above sea level, (Ref. NEBS GR-63) utilizing the host systems designed airflow.

Table 9- Temperature Range Class of operation

Class	**Case Temperature Range**
Standard	0°C through 70°C
Extended	-5°C through 85°C
Industrial	-40°C through 85°C

QSFP-DD is designed to allow for up to 36 modules; stacked, ganged and/or belly-to-belly in a 1U 19" rack, with the appropriate thermal design for cooling/airflow.

7 Management Interface

Editors Note: The Management Interface is still under review by the QSFP-DD MSA members. The final specification will include appropriate updates and remove this editors note.

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This QSFP-DD specification is based on SFF-8636 but with modifications to support an 8-channel module, and as such is not directly backwards compatible with SFF-8636. Some timing requirements are critical, especially for a multi-channel device, so the interface speed may optionally be increased. Byte 00 on the Lower Page or Address 128 Page00 is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map. When a legacy QSFP28 module is inserted into a QSFP-DD port the legacy QSFP memory map (i.e. SFF-8636) must be used. This case is outside the scope of this document.

In some applications, muxing or demuxing may occur in the module. In this specification, all references to channel numbers are based on the electrical connector interface channels, unless otherwise indicated. In cases where a status or control aspect is applicable only to channels after muxing or demuxing has occurred, the status or control is intended to apply to all channels in the mux group, unless otherwise indicated.

7.1 Timing Specification

7.1.1 Introduction

Low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. Detailed electrical specifications are given in SFF-8679 Subsection 5.3. Nomenclature for all registers more than 1 bit long is MSB-LSB.

7.1.2 Management Interface Timing Specification

The timing requirements are shown in Figure 37 and specified in Table 10.
QSFP-DD is positioned to leverage 2-wire timing (Fast Mode devices) to align the use of related cores on host ASICs. The default clock rate is a maximum of 400 kHz with an option to support up to a maximum of 1 MHz. This subsection closely follows the QSFP SFF-8636 specification.

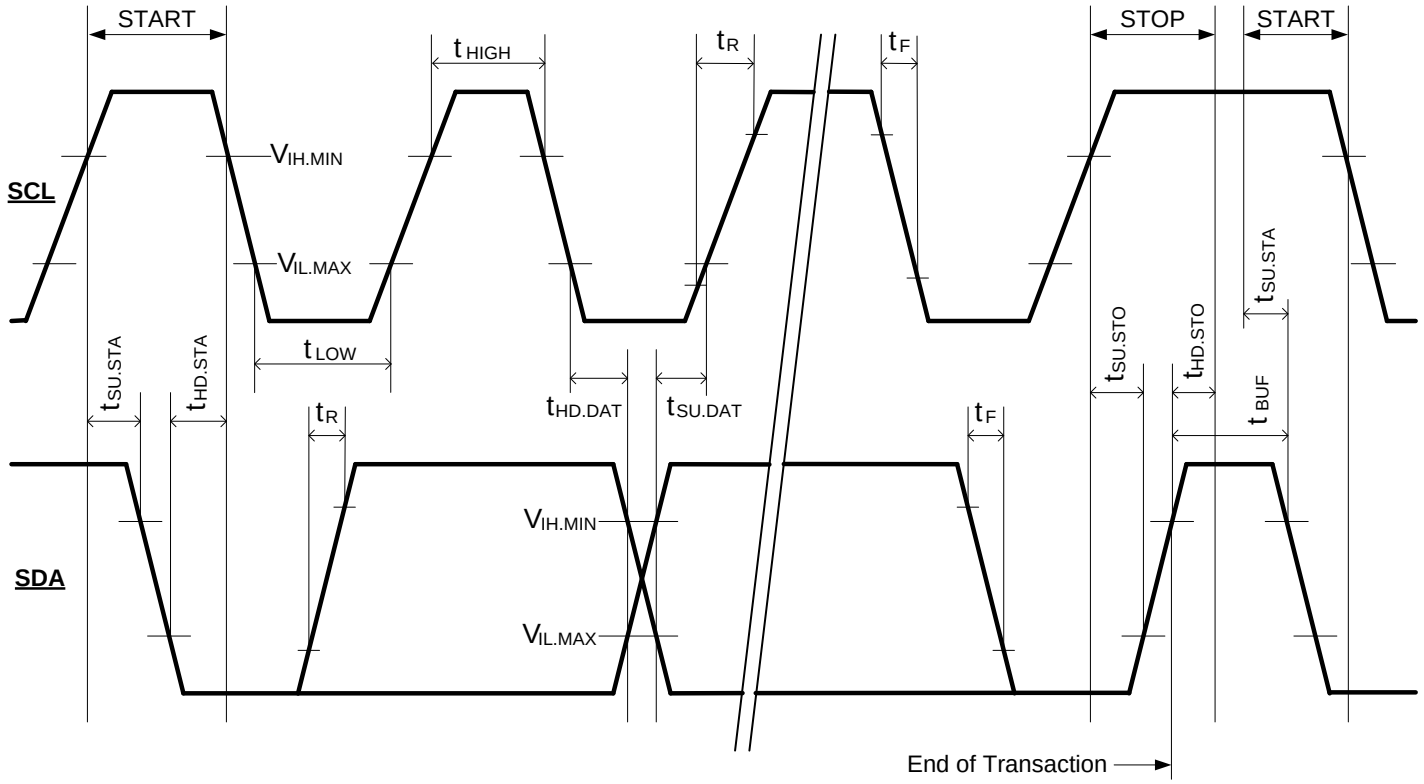


Figure 37: QSFP-DD Timing Diagram

The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h). In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD includes a module select pad, ModSelL. This input (which is pulled high, deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.
Before initiating a 2-wire serial bus communication, the host shall provide setup time on the ModSelL line of all modules on the 2-wire bus. The host shall not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied.

7.1.3 Serial Interface Protocol

7.1.3.1 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module are shown in Table 10. Tradeoffs between Pull up resistor values, bus capacitance and rise time are shown in Figure 38.

Table 10- Management Interface timing parameters

		Fast Mode (400 KHz)		Fast Mode Plus (1 MHz)			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	0	1000	KHz	
Clock Pulse Width Low	tLOW	1.3		0.26		µs	
Clock Pulse Width High	tHIGH	0.6		0.26		µs	
Time bus free before new transmission can start	tBUF	20		1		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		0		µs	
Data In Setup Time	tSU.DAT	0.1		0.1		µs	
Input Rise Time (400kHz)	tR.400		300		120	ns	From (VIL,MAX-0.15) to (VIH, MIN +0.15)
Input Fall Time (400kHz)	tF.400		300		120	ns	From (VIH,MIN + 0.15) to (VIL,MAX – 0.15)
STOP Setup Time	tSU.STO	0.6		0.6		µs	
Aborted sequence – bus release	Deselect _Abort	2		2		ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time[1]	tSU.ModSelL	2		2		ms	ModSelL Setup Time is the setup time on the select lines before the start of a host initiated serial bus sequence.
ModSelL Setup Time[1]	tHD.ModSelL	2		2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module Select status.

Note 1: When the host has determined that module is QSFP-DD, the host can read byte 231 to determine alternate supported ModSelL set up and hold times (see 7.4.2.24 Device Properties).

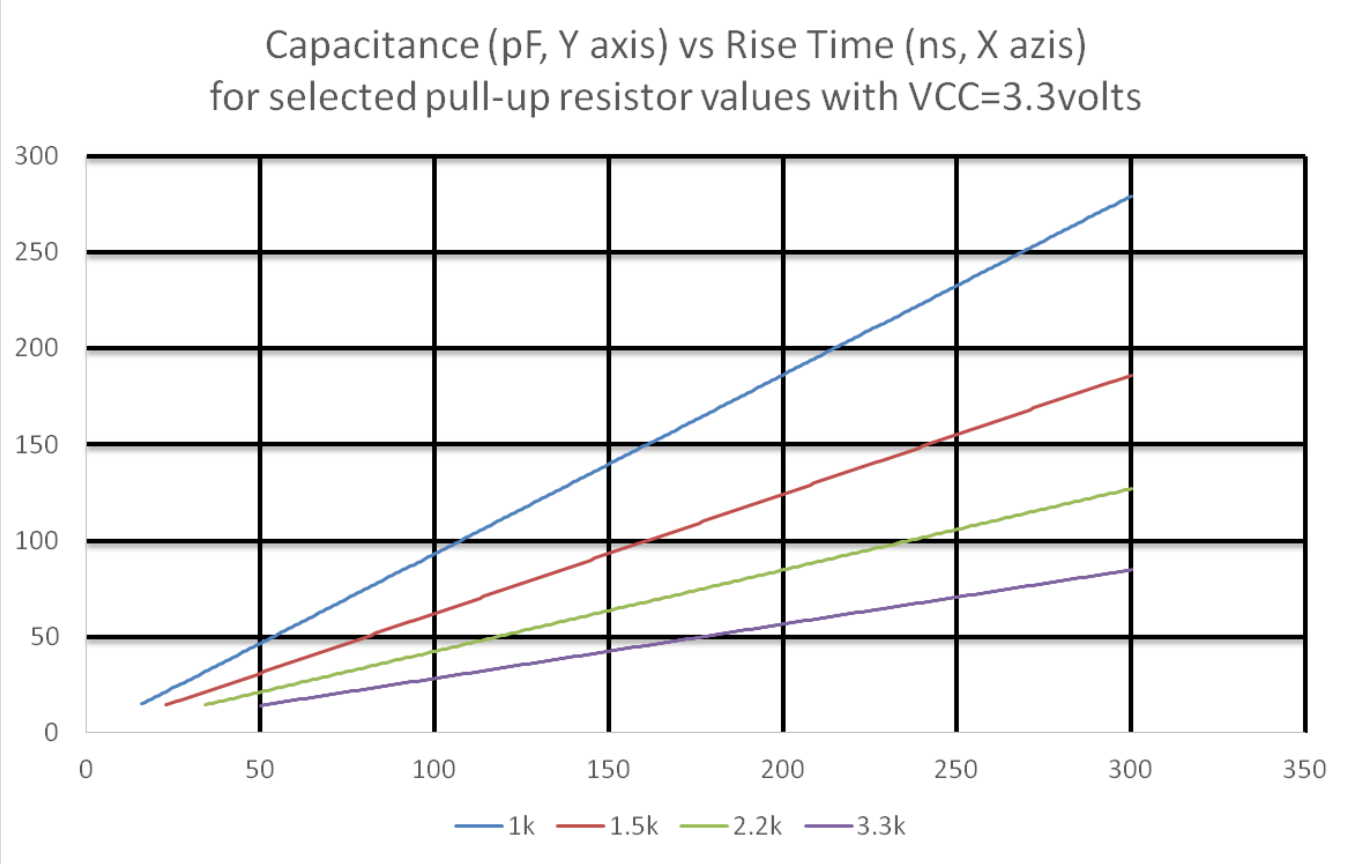


Figure 38: SDA and SCL tradeoffs options for pull-up resistor, bus capacitance and rise/fall times

7.2 Memory Interaction Specifications

QSFP-DD memory transaction timings are given in Table 11.

Table 11- QSFP-DD Memory Specification

Parameter	Symbol	Min	Max	Unit	Conditions
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	µs	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write	tWR		40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50K		cycles	Module Case Temperature = 70^0 C

Table 12- Writable Memory Blocks

Address	# Bytes	Description
Lower Page (Volatile)		
80-88	9	Tx controls
89-91	3	Rx controls
92	1	DataPathEnable
93	1	Power mode control
94-101	8	Rx controls
102-116	15	Hardware Interrupt Masks
117-118	2	Vendor-Specific
119-122	4	Password Change
123-126	4	Password Entry
127	1	Page Select
Upper Page 02h (non-volatile)		
128-255	128	User EEPROM
Upper Page 03h (volatile)		
224-231	8	Tx rate select/application select
232-239	8	Rx rate select/application select
240-251	12	Auxiliary Rx and Tx controls

7.2.1 Timing for Soft Control and Status Functions

Timing for QSFP-DD soft control and status functions are described in Table 13.

Table 13- Timing for QSFP-DD soft control and status functions

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[2] , hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	2		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read[3] operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Deassert Time (optional fast mode)	toff_losf		3	ms	Time from signal present to negation of Rx LOS status bit.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)[1] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)[1] until associated IntL operation resumes
Application or Rate Select Change Time	t_ratesel		100	ms	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Note 1. Measured from the rising edge of SDA in the stop bit of the write transaction					
Note 2. Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.					
Note 3. Measured from the rising edge of SDA in the stop bit of the read transaction					

Squelch and disable timings are defined in Table 14.

Table 14- I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	80	µs	Time from loss of Rx input signal until the squelched output condition is reached. See Subsection 4.1.3.1.
Rx Squelch Deassert Time	toff_Rxsq	80	µs	Time from resumption of Rx input signals until normal Rx output condition is reached. See subsection 4.1.3.1.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached. See subsection 4.1.3.2.
Tx Squelch Deassert Time	toff_Txsq	400	ms	Time from resumption of Tx input signals until normal Tx output condition is reached. See subsection 4.1.3.2.
Tx Disable Assert Time	ton_txdis	100	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal
Tx Disable Deassert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Tx Disable Deassert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable Deassert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable Deassert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled
Note 1: Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction				

7.3 QSFP-DD Initialization State Machine

The QSFP-DD Initialization state machine is defined in Figure 39 to formalize interactions between the host and module during the module power up sequence. The state machine is applicable to all QSFP-DD modules and cable assemblies, whether passive or active.

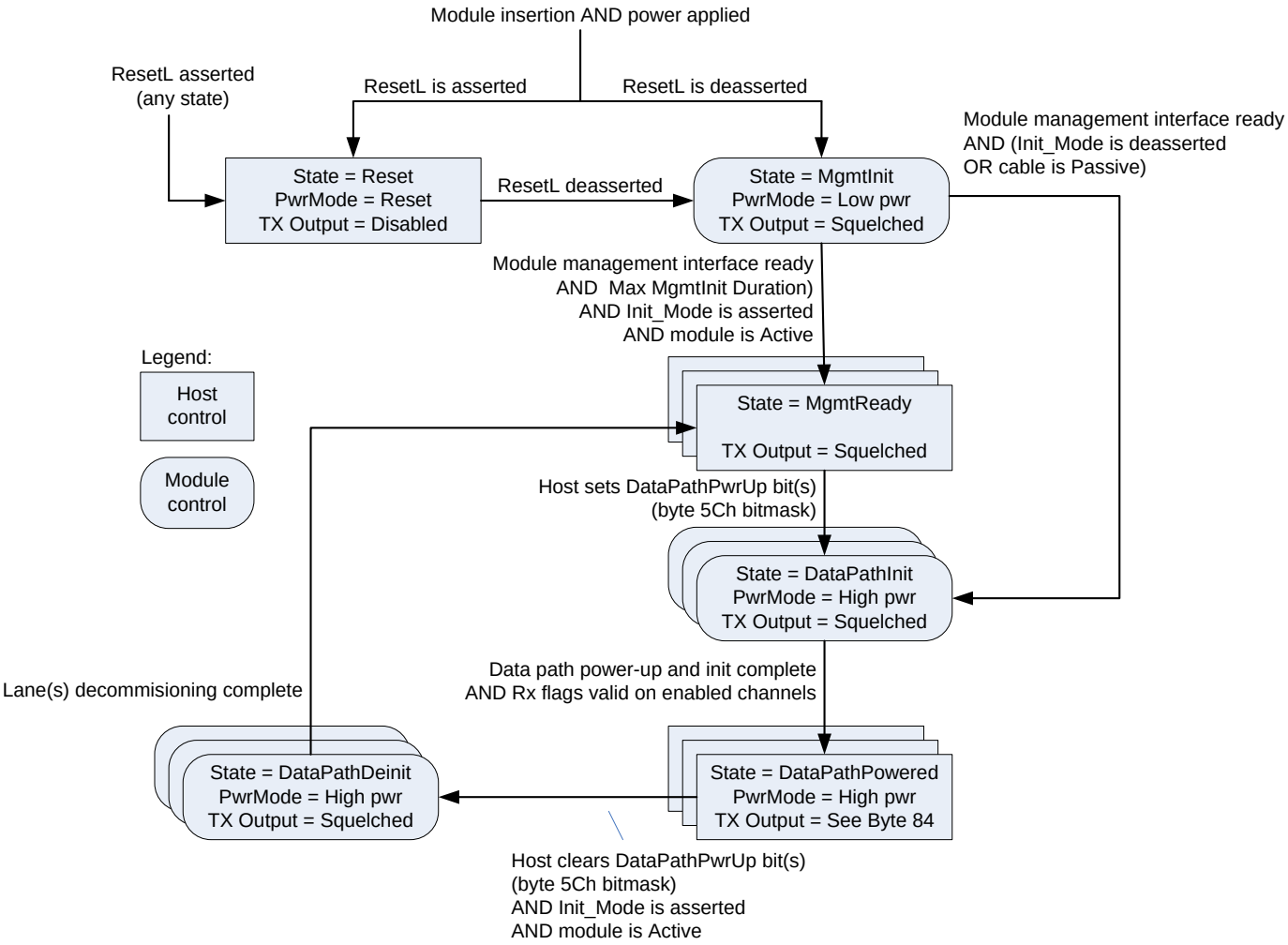


Figure 39 Initialization State Machine

States with a rectangular outline are states where the host is in control of initialization activities. In order for the state machine to progress out of these states, the host must initiate an action through the memory map or through one of the sideband signals. The duration of host control states is unbounded.

States with an oval outline are transient states where the module is in control of initialization activities. These module control states have an implementation-dependent maximum duration as reported in the Max DataPathInit Duration and Max TX DataPathDeinit Duration registers in the memory map. In general, host interactions with the module should be minimized during these transient states, with memory map accesses limited to read-only static register content. Dynamic register content is unreliable during transient states. When the host has caused the transition to a transient state on one or more electrical channels of the module, the module may ignore requests to transition other electrical channels to any transient state until the initially requested transient state has completed.

States that contain stacked boxes are electrical channel-dependent states, to support breakout applications. For these states, each electrical channel in the module may be in a different state at the same time. The memory map contains an Initialization State register to report the current state of each electrical channel. Some transient states may be so short that the State Indicators register (see Table 17) is not updated. Refer to Subsection 7.4.1.3 State Indicators) for the definition of the State Indicators register encodings and Subsection 7.6.2.26 for transient state duration encodings.
All active modules shall enter Low Power Mode upon insertion or assertion, power up or assertion of ResetL unless the InitMode signal is deasserted. When active modules are in low power mode, the module receiver high speed signal outputs shall be quiescent and the transmitter optical outputs shall be disabled. All passive copper cable assemblies shall be fully functional immediately upon insertion.

The host may use the InitMode signal to define the power up sequence to be used. If the InitMode signal is asserted, the module shall follow the host software-controlled power-up sequence. If the InitMode signal is de-asserted, the module bypasses MgmtReady and DataPathInit and proceeds immediately to High Power Mode in the DataPathPowered state, without host software interaction. In this scenario, the module shall use default settings in the memory map to identify initialization parameters and shall perform all data path initialization activities, as defined in DataPathInit, prior to entering DataPathPowered and without notifying the host upon completion. The host shall not change the state of InitMode while a module is present, unless the module is in the Reset state.

7.3.1 MgmtInit State

The MgmtInit state is a module-wide transient state that is entered any time the module is brought out of Reset, due to deassertion of the ResetL signal or upon initial insertion and application of power. The MgmtInit state is applicable to both active modules and passive copper cable assemblies.

During this state, the module shall initialize the management interface and configure the memory map for access by the host. The module may perform limited power-up of the high-speed data path circuitry, however the module shall remain in Low Power mode throughout this state and all module TX and RX data path outputs shall be squelched. The module may ignore all 2-wire serial interface transactions while in this state.

The module shall not assert IntL during MgmtInit. Interrupt flags shall confirm to Flag Class 1, defined in Section 7.5.7. If catastrophic module faults occur, the module shall transition immediately to the next state to report the fault. The module shall report all valid non-catastrophic faults and warnings that remain valid after transitioning to the next state.
Before the module exits the MgmtInit state, all memory map register locations shall be set to their power-on defaults. The module shall have completed MgmtInit in accordance with Max Mgmtinit Duration as defined in Table 13. The duration of the MgmtInit state, Max MgmtInit Duration, is the time from power on (defined as the instant when supply voltages reach and remain at or above the minimum level specified in Section 4.2), hot plug, or the rising edge of ResetL until the module has configured the memory map to default conditions and activated the management interface.

Upon completion of MgmtInit, the next state depends on the cable type and the InitMode signal. In all cases, all electrical channels shall transition to the same state as defined by the following rules. For passive copper cable assemblies the next state is DatPathInit. For active modules when the InitMode signal is in the asserted state, the next state is MgmtReady. Note that modules with a very short DataPathInit Duration may not generate IntL.

7.3.2 MgmtReady State

The MgmtReady state is a electrical channel-specific host-controlled state. During this state, the host may configure the module using the management interface and memory map. Some examples of configuration activities include reading the ID and device property fields, setting CDR and other channel attributes and configuration of monitor masks.

Details of host-module interactions in the MgmtReady State are implementation dependent and are outside the scope of this specification.

Upon entry into the MgmtReady state, the module shall set the Initialization State register to the MgmtReady state for the applicable electrical channel(s), set the State Changed flag and any applicable fault and warning flags that are valid after transitioning to the MgmtReady state, and assert the IntL signal. The host shall read the State Changed flag along with all other fault and warning flags to deassert the IntL signal.

If all electrical channels are in the MgmtReady state, the module shall be in Low Power Mode. Otherwise the module shall be in High Power Mode. Before exiting Low Power Mode (by asserting any DataPathPwrUp bit) the host shall program all the control registers, especially Tx Disable and Rx Output Disable, to the host's desired configuration.

For all channels in the MgmtReady state, the outputs shall remain quiescent until the DataPathPwrUp bits for those channels are set.

Interrupt Flag Class 1 shall be applied throughout MgmtReady for all electrical channels in the MgmtReady state.

When the host has completed module configuration, the host may initiate the data path on one or more electrical channels by setting the applicable bits in the DataPathPwrUp register in the memory map. Prior to exit from this state, the host shall enable all applicable host transmitters and provide compliant signals, so that the module can configure TX electrical input circuitry while in the DataPathInit state.

7.3.3 DataPathInit State

The DataPathInit state is a per-electrical channel transient state where the module powers up the TX and RX high speed data path electronics and applies module configuration settings defined in the module memory map. Example TX activities during this state include adaptation of module CTLE and TX CDR lock. Example RX activities during this state include arming of the RX CDR and application of RX output amplitude and emphasis. Note that input data may not be present on the RX input, and so CDRs may remain unlocked and the module output may remain squelched. The duration of the DataPathInit state, DataPathInit Duration, is the time from the rising edge of the SDA stop bit of the DataPathPwrUp bit write transaction to the assertion of the initialization completed IntL (IntL Vout = Vol), both times are observed at the module. The maximum duration of the DataPathInit state shall be identified by the module vendor in the Max_DataPathInit_Duration register. Encodings for Max DataPathInit Duration are defined in Table 40.

Upon entry into the DataPathInit state, the module shall enter High Power mode (if not already in High Power Mode) and set the applicable electrical channel(s) of the Initialization_State register to the DataPathInit state.

For all channels in the DataPathInit state, the outputs shall remain quiescent throughout DataPathInit. The host shall minimize 2-wire serial transactions while in this state.

Dynamic memory map content may be unreliable while in this state and should not be read or written.

Interrupt Flag Class 1 shall be applied throughout DataPathInit for all electrical channels in the DataPathInit state.

When the module has completed power-up and initialization of the applicable electrical channel(s) TX high-speed data path circuitry, power-up of the RX high-speed data path circuitry, and all TX and RX data path flags, alarms, and warnings are valid, the module shall transition to the DataPathPowered state.

7.3.4 DataPathPowered State

The DataPathPowered state is a electrical channel-specific host-controlled state. Electrical channels that are in the DataPathPowered state are considered fully initialized and ready to transmit live traffic.

Upon entry into the DataPathPowered state, the module shall set the Initialization State register to the DataPathPowered state, set the State Changed flag and any valid fault and warning flags and assert the IntL signal.

Interrupt Flag Class 2 shall be applied throughout DataPathPowered for all electrical channels in the DataPathInit state.

For active modules, the module shall be in High Power Mode when any electrical channel is in the DataPathPowered State. The host may enable and disable TX outputs at any time for electrical channels in the DataPathPowered State. Note: Where two or more electrical channels are multiplexed to form a single optical channel, the associated optical channels shall be squelched whenever any of the associated electrical channels are disabled. Active module electrical channels transition to the DataPathDeinit state when the host clears the applicable bits in the DataPathPwrUp register in the memory map, but only if the InitMode signal is in the asserted state. For passive modules, the module shall remain in Low Power Mode throughout the DataPathPowered State.

7.3.5 DataPathDeinit State

The DataPathDeinit state is a channel-specific transient state that is entered when the host deasserts the DataPathPwrUp bit for the channel of interest. If, upon entry into DataPathDeinit, all bits of the DataPathPwrUp register are clear, the module shall return to Low Power Mode.

Upon entry into the DataPathDeinit state, the module shall set the applicable electrical channels in the State Indicators register to the DataPathDeinit state.

The host shall minimize 2-wire serial transactions while in this state. Dynamic memory map content may be unreliable for channels in this state and should not be read or written.

Interrupt Flag Class 1 shall be applied throughout DataPathDeinit for all electrical channels in the DataPathInit state.

When the module has completed applicable power down activities, the channel shall transition to the MgmtReady state.

The maximum duration of the DataPathDeinit state shall be identified by the module vendor in the Max DataPathDeinit Duration register (Table 39). Encodings for Max DataPathDeinit Duration are defined in Table 40.

7.3.6 Reset State

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. The Mgmt Init state time (Max MgmtInit Duration) starts on the rising edge after the low level on the ResetL pin is released.
During the execution of a reset (Max MgmtInit Duration) the host shall disregard all status bits until the module indicates a completion of the Mgmt Init state. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset. The Reset state can be entered from any state by assertion of the ResetL signal. For passive copper cables, holding the EEPROM in reset is optional. The TX output for active modules shall be disabled throughout the Reset state. Management interface transactions initiated by the host during the Reset state may be ignored by the module. The Reset state can only be exited by deassertion of the ResetL signal. Upon exit from the Reset state, the module shall enter the MgmtInit state.

7.3.7 Interrupt Flag Applicability Per State

Some module interrupt flags are generated by the state machine, but the majority of the flags are triggered by other sources. The host may choose to mask any flag by setting the appropriate mask bits during the MgmtReady or DataPathPowered states.
Since many states in the state machine are electrical channel-specific and different electrical channels in the module may be in different states at the same time, interrupt flags are grouped by class to define a simplistic mechanism for defining which flags are applicable in which scenarios. For flags that are module-wide, the highest numbered Flag Class across all module electrical channels shall apply. For flags that are electrical channel-specific, the Flag Class for that electrical channel’s state shall apply.

Table 15- Interrupt Flag Classes

Interrupt Flag Class	**Flags Permitted**
Flag Class 0	All Flags suppressed
Flag Class 1	Data path flags suppressed Module flags permitted
Flag Class 2	All Flags permitted

7.4 QSFP-DD Memory Map

This subsection defines the Memory Map for QSFP-DD Module used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP-DD devices. The interface has been designed largely after the CDFP MSA which in turn was derived from QSFP. The memory map has been changed in order to accommodate 8 electrical channels and limit the required memory space. The single address approach is used as found in QSFP. Paging is used in order to enable time critical interactions between host and module.

The structure of the memory is shown in Figure 40. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 40 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides a user read/write space. The lower page and upper page 00 are always implemented. Page 03 is required if byte 2, bit 2 in the lower page is low. See Table 36 for details regarding the declaration of optional upper pages 01 and 02.

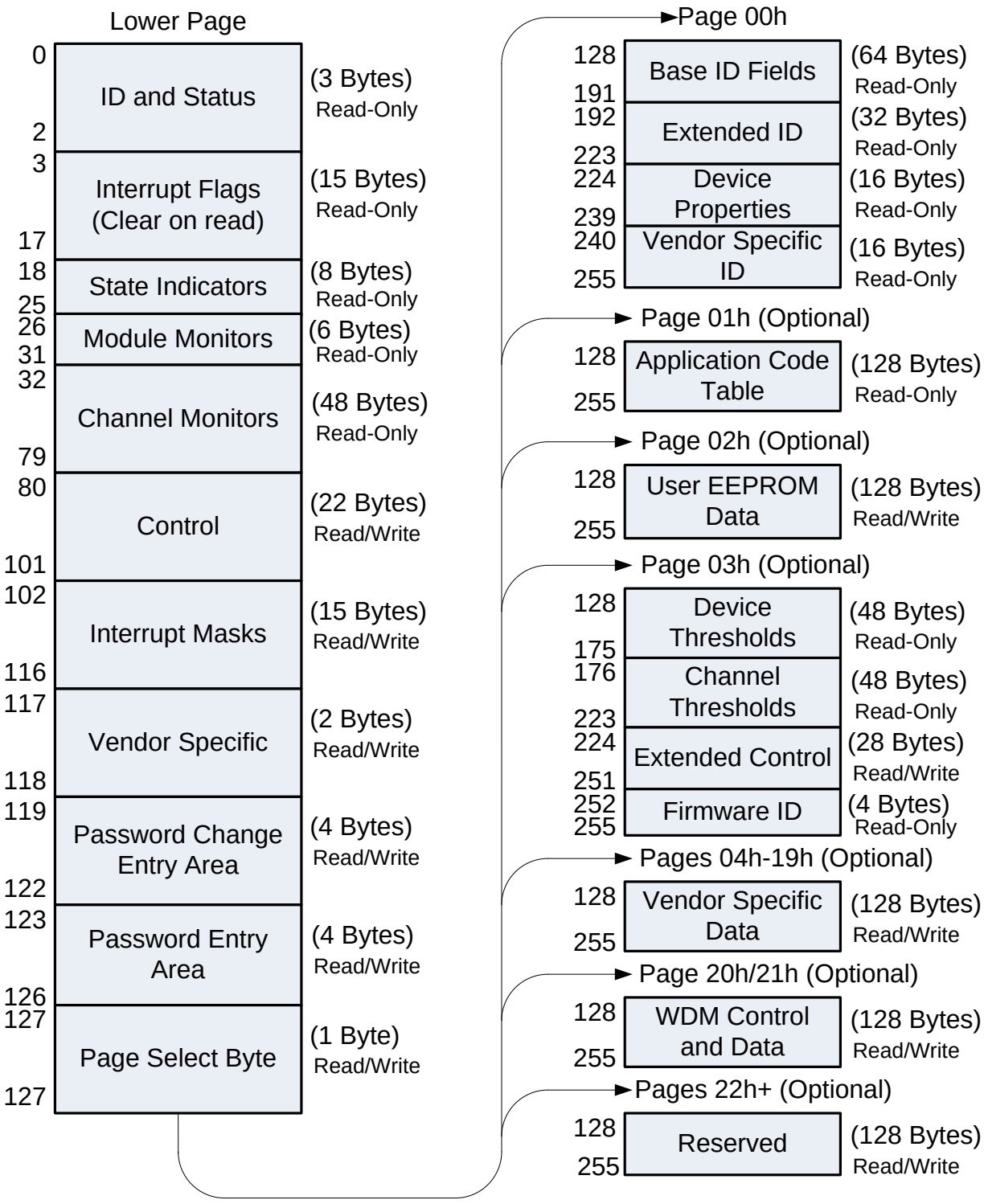


Figure 40: QSFP-DD Memory Map

7.4.1 Lower Page 00h

The lower 128 bytes of the two-wire serial bus address space is used to access a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed.

The lower page is subdivided into several areas as illustrated in the following table:

Table 16- Lower Page Overview (Lower Page)

Address	Description	Type
0 – 2	Id and Status (3 bytes)	Read-only
3 – 17	Interrupt Flags (15 bytes)	Read-only
18 - 25	State Indicators (8 bytes)	Read-only
26 – 31	Module card Monitors (6 bytes)	Read-only
32 – 79	Channel Monitors (48 bytes)	Read-only
80 – 101	Control Fields (22 bytes)	Read/Write
102 – 116	Interrupt Flag Masks (15 bytes)	Read/Write
117 - 118	Reserved	Read/Write
119 – 122	Password Change Area (4 bytes)	Write-Only
123 – 126	Password Entry Area (4 bytes)	Write-Only
127	Page Select Byte	Read/Write

7.4.1.1 ID and Status

Table 17- Identifier and Status Summary (Lower Page)

Byte	Bits	Name	Description	Type
0 00h	All	Identifier	Identifier - Type of Serial Module - See SFF-8024. A value of 18h indicates a QSFP-DD transceiver.	RO Rqrd.
1 01h	All	Version Id	Identifier – Version of QSFP-DD Serial Module Specification; the upper nibble is the whole number part and the lower nibble is the decimal part. Example: 01h indicates version 0.1, 21h indicates version 2.1.	RO Rqrd.
2 02h	7-4	Reserved		RO Rqrd.
	3	Reserved		
	2	Flat_mem	Upper memory flat or paged. Coded 0 for paged memory; coded 1 for flat memory (only page 00h implemented)	
	1	Interrupt	"Digital state of the IntL Interrupt output pin 1 = IntL not asserted, 0 = IntL asserted. Default = 1	
	0	DataNotReady	Indicates module card has not yet achieved power up and monitor data is not ready. Bit remains high until monitor data is ready to be read at which time the device sets the bit low.	

The DataNotReady bit is high during module power up and prior to a valid suite of monitor readings. Once all monitor readings are valid, the bit is set low until the device is powered down or reset.

7.4.1.2 Interrupt Flags

A portion of the memory map (bytes 3 through 16), forms a flags field. Within this field, the status of LOS and Tx Fault as well as alarms and warnings for the various monitored items is reported. An RX LOS on an optical channel may affect multiple electrical RX channels. This occurs when electrical channels are de-multiplexed from a single optical channel. (See Section 5.10) If a TX LOS is detected on any electrical channel associated with an optical channel the optical channel will be squelched. If a monitor with associated alarm and/or warning thresholds is implemented the associated flags and flag masks must also be implemented. For normal operation and default state, the bits in this field have the value of 0b. For the defined conditions of LOS, LOL, Tx Fault, module and channel alarms and warnings, the appropriate bit or bits are set, value = 1b. Once asserted, the bits remained set (latched) until cleared by a read operation that includes the affected bit or reset by the ResetL pin. If the corresponding mask bit is not set (see Table 30), IntL is also asserted at the onset of the condition and remains asserted until all unmasked interrupt flags have been read by the host. After being read and cleared, the bit may be set again if the condition persists; this does not cause IntL to be asserted again. The Interrupt Flags are defined in Table 18.

Table 18- Interrupt Flags (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
3	7	L-Rx8 LOS	Latched Rx LOS indicator, channel 8	RO
03h	6	L-Rx7 LOS	Latched Rx LOS indicator, channel 7	Opt.
	5	L-Rx6 LOS	Latched Rx LOS indicator, channel 6	
	4	L-Rx5 LOS	Latched Rx LOS indicator, channel 5	
	3	L-Rx4 LOS	Latched Rx LOS indicator, channel 4	
	2	L-Rx3 LOS	Latched Rx LOS indicator, channel 3	
	1	L-Rx2 LOS	Latched Rx LOS indicator, channel 2	
	0	L-Rx1 LOS	Latched Rx LOS indicator, channel 1	
4	7	L-Tx8 LOS	Latched Tx LOS indicator, channel 8	RO
04h	6	L-Tx7 LOS	Latched Tx LOS indicator, channel 7	Opt.
	5	L-Tx6 LOS	Latched Tx LOS indicator, channel 6	
	4	L-Tx5 LOS	Latched Tx LOS indicator, channel 5	
	3	L-Tx4 LOS	Latched Tx LOS indicator, channel 4	
	2	L-Tx3 LOS	Latched Tx LOS indicator, channel 3	
	1	L-Tx2 LOS	Latched Tx LOS indicator, channel 2	
	0	L-Tx1 LOS	Latched Tx LOS indicator, channel 1	
5	7	L-Rx8 CDR LOL	Latched Rx CDR LOL indicator, channel 8	RO
05h	6	L-Rx7 CDR LOL	Latched Rx CDR LOL indicator, channel 7	Opt.
	5	L-Rx6 CDR LOL	Latched Rx CDR LOL indicator, channel 6	
	4	L-Rx5 CDR LOL	Latched Rx CDR LOL indicator, channel 5	
	3	L-Rx4 CDR LOL	Latched Rx CDR LOL indicator, channel 4	
	2	L-Rx3 CDR LOL	Latched Rx CDR LOL indicator, channel 3	
	1	L-Rx2 CDR LOL	Latched Rx CDR LOL indicator, channel 2	
	0	L-Rx1 CDR LOL	Latched Rx CDR LOL indicator, channel 1	
6	7	L-Tx8 CDR LOL	Latched Tx CDR LOL indicator, channel 8	RO
06h	6	L-Tx7 CDR LOL	Latched Tx CDR LOL indicator, channel 7	Opt.
	5	L-Tx6 CDR LOL	Latched Tx CDR LOL indicator, channel 6	
	4	L-Tx5 CDR LOL	Latched Tx CDR LOL indicator, channel 5	
	3	L-Tx4 CDR LOL	Latched Tx CDR LOL indicator, channel 4	
	2	L-Tx3 CDR LOL	Latched Tx CDR LOL indicator, channel 3	
	1	L-Tx2 CDR LOL	Latched Tx CDR LOL indicator, channel 2	
	0	L-Tx1 CDR LOL	Latched Tx CDR LOL indicator, channel 1	
7	7	L-Tx8 Fault	Latched Tx fault indicator, channel 8	RO
07h	6	L-Tx7 Fault	Latched Tx fault indicator, channel 7	Opt.
	5	L-Tx6 Fault	Latched Tx fault indicator, channel 6	for

	4	L-Tx5 Fault	Latched Tx fault indicator, channel 5	PC,AC, AO. R for SM
	3	L-Tx4 Fault	Latched Tx fault indicator, channel 4	
	2	L-Tx3 Fault	Latched Tx fault indicator, channel 3	
	1	L-Tx2 Fault	Latched Tx fault indicator, channel 2	
	0	L-Tx1 Fault	Latched Tx fault indicator, channel 1	
8 08h	7	L-Temp High Alarm	Latched high temperature alarm flag	RO Opt.
	6	L-Temp Low Alarm	Latched low temperature alarm flag	
	5	L-Temp High Warning	Latched high temperature warning flag	
	4	L-Temp Low Warning	Latched low temperature warning flag	
	3-0	Reserved		
	7	L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm flag	
	6	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	5-4	Reserved		
9 09h	3	L-TEC Current High Alarm	Latched TEC supply current high alarm flag	
	2	L-TEC Current Fault	Latched TEC supply current fault alarm flag	
	1	L-Adaptation Complete	Asserted (one) after adaptive equalization has completed. Returns to Zero when read; does not reassert unless re-triggered.	RO Opt.
	0	L-State Changed Flag	Asserted (one) after a change of state has been completed. Returns to Zero when read; does not reassert unless re-triggered.	RO Opt.
	7	L-Rx8 Power Low Warning	Latched low Rx power warning flag, channel 8	
	6	L-Rx7 Power Low Warning	Latched low Rx power warning flag, channel 7	
	5	L-Rx6 Power Low Warning	Latched low Rx power warning flag, channel 6	
10 0Ah	4	L-Rx5 Power Low Warning	Latched low Rx power warning flag, channel 5	
	3	L-Rx4 Power Low Warning	Latched low Rx power warning flag, channel 4	
	2	L-Rx3 Power Low Warning	Latched low Rx power warning flag, channel 3	RO Opt.
	1	L-Rx2 Power Low Warning	Latched low Rx power warning flag, channel 2	
	0	L-Rx1 Power Low Warning	Latched low Rx power warning flag, channel 1	RO Opt.
	7	L-Rx8 Power Low Alarm	Latched low Rx power alarm flag, channel 8	
	6	L-Rx7 Power Low Alarm	Latched low Rx power alarm flag, channel 7	
	5	L-Rx6 Power Low Alarm	Latched low Rx power alarm flag, channel 6	
11 0Bh	4	L-Rx5 Power Low Alarm	Latched low Rx power alarm flag, channel 5	
	3	L-Rx4 Power Low Alarm	Latched low Rx power alarm flag, channel 4	
	2	L-Rx3 Power Low Alarm	Latched low Rx power alarm flag, channel 3	RO Opt.
	1	L-Rx2 Power Low Alarm	Latched low Rx power alarm flag, channel 2	
	0	L-Rx1 Power Low Alarm	Latched low Rx power alarm flag, channel 1	RO Opt.
	7	L-Rx8 Power High Alarm	Latched high Rx power alarm flag, channel 8	
	6	L-Rx7 Power High Alarm	Latched high Rx power alarm flag, channel 7	
	5	L-Rx6 Power High Alarm	Latched high Rx power alarm flag, channel 6	
12 0Ch	4	L-Rx5 Power High Alarm	Latched high Rx power alarm flag, channel 5	
	3	L-Rx4 Power High Alarm	Latched high Rx power alarm flag, channel 4	
	2	L-Rx3 Power High Alarm	Latched high Rx power alarm flag, channel 3	RO Opt.
	1	L-Rx2 Power High Alarm	Latched high Rx power alarm flag, channel 2	
	0	L-Rx1 Power High Alarm	Latched high Rx power alarm flag, channel 1	RO Opt.
	7	L-Tx8 Bias Low Alarm	Latched low Tx bias alarm flag, channel 8	
	6	L-Tx7 Bias Low Alarm	Latched low Tx bias alarm flag, channel 7	
	5	L-Tx6 Bias Low Alarm	Latched low Tx bias alarm flag, channel 6	
13 0Dh	4	L-Tx5 Bias Low Alarm	Latched low Tx bias alarm flag, channel 5	
	3	L-Tx4 Bias Low Alarm	Latched low Tx bias alarm flag, channel 4	
	2	L-Tx3 Bias Low Alarm	Latched low Tx bias alarm flag, channel 3	RO Opt.
	1	L-Tx2 Bias Low Alarm	Latched low Tx bias alarm flag, channel 2	
	0	L-Tx1 Bias Low Alarm	Latched low Tx bias alarm flag, channel 1	RO Opt.
14	7	L-Tx8 Bias High Alarm	Latched high Tx bias alarm flag, channel 8	

0Eh	6	L-Tx7 Bias High Alarm	Latched high Tx bias alarm flag, channel 7	
	5	L-Tx6 Bias High Alarm	Latched high Tx bias alarm flag, channel 6	
	4	L-Tx5 Bias High Alarm	Latched high Tx bias alarm flag, channel 5	
	3	L-Tx4 Bias High Alarm	Latched high Tx bias alarm flag, channel 4	
	2	L-Tx3 Bias High Alarm	Latched high Tx bias alarm flag, channel 3	RO
	1	L-Tx2 Bias High Alarm	Latched high Tx bias alarm flag, channel 2	Opt.
	0	L-Tx1 Bias High Alarm	Latched high Tx bias alarm flag, channel 1	RO
	7	L-Tx8 Power Low Alarm	Latched low Tx power alarm flag, channel 8	Opt.
	6	L-Tx7 Power Low Alarm	Latched low Tx power alarm flag, channel 7	
	5	L-Tx6 Power Low Alarm	Latched low Tx power alarm flag, channel 6	
15	4	L-Tx5 Power Low Alarm	Latched low Tx power alarm flag, channel 5	
0Fh	3	L-Tx4 Power Low Alarm	Latched low Tx power alarm flag, channel 4	
	2	L-Tx3 Power Low Alarm	Latched low Tx power alarm flag, channel 3	RO
	1	L-Tx2 Power Low Alarm	Latched low Tx power alarm flag, channel 2	Opt.
	0	L-Tx1 Power Low Alarm	Latched low Tx power alarm flag, channel 1	RO
	7	L-Tx8 Power High Alarm	Latched high Tx power alarm flag, channel 8	Opt.
	6	L-Tx7 Power High Alarm	Latched high Tx power alarm flag, channel 7	
	5	L-Tx6 Power High Alarm	Latched high Tx power alarm flag, channel 6	
16	4	L-Tx5 Power High Alarm	Latched high Tx power alarm flag, channel 5	
10h	3	L-Tx4 Power High Alarm	Latched high Tx power alarm flag, channel 4	
	2	L-Tx3 Power High Alarm	Latched high Tx power alarm flag, channel 3	RO
	1	L-Tx2 Power High Alarm	Latched high Tx power alarm flag, channel 2	Opt.
	0	L-Tx1 Power High Alarm	Latched high Tx power alarm flag, channel 1	
17 11h	All	Reserved (PAM4/WDM)		

7.4.1.3 State Indicators

The state indicators hold the unlatched state of the various channel states and single-bit sensors. Passive copper cables shall use an encoding of 10b for all channels. The encoding of the state indicators is shown in Table 18. The state indicators follow the state machine in Figure 40. See Table 40State Duration Encoding for the delay times for transient states.

Table 19- State Indicators (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
18 12h	7-6	Channel 4 State	Encoded state-machine state for channel 4	RO Opt.
	5-4	Channel 3 State	Encoded state-machine state for channel 3	
	3-2	Channel 2 State	Encoded state-machine state for channel 2	
	1-0	Channel 1 State	Encoded state-machine state for channel 1	
19 13h	7-6	Channel 8 State	Encoded state-machine state for channel 8	RO Opt.
	5-4	Channel 7 State	Encoded state-machine state for channel 7	
	3-2	Channel 6 State	Encoded state-machine state for channel 6	
	1-0	Channel 5 State	Encoded state-machine state for channel 5	
20	7-1	Reserved		
14h	0	TEC Stable	Unlatched TEC stability indicator (if any)	
21-25 15h-19h	All	Vendor Specific		

Table 20- Channel State register encoding

Encoding	State
00b	MgmtReady
01b	DataPathInit
10b	DataPathPowered Passive cable shall use this encoding for all channels
11b	DataPathDeinit

7.4.1.4 Module Monitors

Optional real time monitoring for the module includes an internal module temperature, supply voltage, and monitoring for each transmit and receive channel. Measured parameters are reported in 16-bit data fields, i.e. two concatenated bytes, most-significant byte (MSB) first. To guarantee coherency of the diagnostic monitoring data, the host should retrieve any multi-byte fields from the diagnostic monitoring data structure by the use of a single multi-byte read sequence across the two-wire serial interface.

Internally measured device temperatures are represented as a 16-bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of -128 C to +128 C that is considered valid in the range specified in the device datasheet. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over the specified operating temperature and voltage.

Internally measured module 3.3 volts supply voltage is represented as a 16-bit unsigned integer with the voltage defined as the full 16-bit value (0 – 65535) with LSB equal to 100 uVolt, yielding a total measurement range of 0 to +6.55 Volts. Accuracy is vendor specific but must be better than ±3% of the manufacturer’s nominal value over specified operating temperature and voltage.

Table 21- Module Monitors (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
26 1Ah	All	Temperature1 MSB	Internally measured temperature	RO Opt. for PC,AC, AO. Rqrd. for SM
27 1Bh	All	Temperature1 LSB		
29-28 1D-1Ch	All	Reserved		RO Opt.
30 1Eh	All	Supply 3.3-volt MSB	Internally measured supply voltage, 3.3 volt input voltage in 100µV units	RO Opt.
31 1Fh	All	Supply 3.3-volt LSB		

7.4.1.5 Channel Monitors

Real time channel monitoring is performed for each transmit and receive channel and includes Rx optical input power and Tx bias current. Alarm and warning threshold values should be interpreted in the same manner as real time 16-bit data.

Measured RX received optical power is in mW and can represent either average received power or OMA depending upon how bit 3 of byte 220 (upper memory page 00h) is set. Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 - 65535) with LSB equal to 0.1 µW, yielding a total measurement range of 0 to 6.5535 mW (approx. -40 to +8.2 dBm).

Measured Tx bias current is in mA and are represented as a 16-bit unsigned integer with the current defined as the full 16-bit value (0 – 65535) with LSB equal to 2 µA, yielding a total measurement range of 0 to 131 mA.

Table 22- Channel Monitors (Lower Page, active modules only)

Byte	Bit	Name	Description	Type
32, 20h	All	Rx1 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 1	RO Opt.
33, 21h	All	Rx1 Power LSB		
34, 22h	All	Rx2 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 2	RO Opt.
35, 23h	All	Rx2 Power LSB		
36, 24h	All	Rx3 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 3	RO Opt.
37, 25h	All	Rx3 Power LSB		
38, 26h	All	Rx4 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 4	RO Opt.
39, 27h	All	Rx4 Power LSB		
40, 28h	All	Rx5 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 5	RO Opt.
41, 29h	All	Rx5 Power LSB		
42, 2Ah	All	Rx6 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 6	RO Opt.
43, 2Bh	All	Rx6 Power LSB		
44, 2Ch	All	Rx7 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 7	RO Opt.
45, 2Dh	All	Rx7 Power LSB		
46, 2Eh	All	Rx8 Power MSB	Rx Light Input Monitor in 0.1µW units, channel 8	RO Opt.
47, 2Fh	All	Rx8 Power LSB		
48, 30h	All	Tx1 Bias MSB	Internally measured Tx bias current, channel 1	RO Opt.
49, 31h	All	Tx1 Bias LSB		
50, 32h	All	Tx2 Bias MSB	Internally measured Tx bias current, channel 2	RO Opt.
51, 33h	All	Tx2 Bias LSB		
52, 34h	All	Tx3 Bias MSB	Internally measured Tx bias current, channel 3	RO Opt.
53, 35h	All	Tx3 Bias LSB		
54, 36h	All	Tx4 Bias MSB	Internally measured Tx bias current, channel 4	RO Opt.
55, 37h	All	Tx4 Bias LSB		
56, 38h	All	Tx5 Bias MSB	Internally measured Tx bias current, channel 5	RO Opt.
57, 39h	All	Tx5 Bias LSB		
58, 3Ah	All	Tx6 Bias MSB	Internally measured Tx bias current, channel 6	RO Opt.
59, 3Bh	All	Tx6 Bias LSB		
60, 3Ch	All	Tx7 Bias MSB	Internally measured Tx bias current, channel 7	RO Opt.
61, 3Dh	All	Tx7 Bias LSB		
62, 3Eh	All	Tx8 Bias MSB	Internally measured Tx bias current, channel 8	RO Opt.
63, 3Fh	All	Tx8 Bias LSB		
64, 40h	All	Tx1 Power MSB	Internally measured Tx power, channel 1	RO Opt.
65, 41h	All	Tx1 Power LSB		
66, 42h	All	Tx2 Power MSB	Internally measured Tx power, channel 2	RO Opt.
67, 43h	All	Tx2 Power LSB		
68, 44h	All	Tx3 Power MSB	Internally measured Tx power, channel 3	RO Opt.
69, 45h	All	Tx3 Power LSB		
70, 46h	All	Tx4 Power MSB	Internally measured Tx power, channel 4	RO

71, 47h	All	Tx4 Power LSB		Opt.
72, 48h	All	Tx5 Power MSB	Internally measured Tx power, channel 5	RO
73, 49h	All	Tx5 Power LSB		Opt.
74, 4Ah	All	Tx6 Power MSB	Internally measured Tx power, channel 6	RO
75, 4Bh	All	Tx6 Power LSB		Opt.
76, 4Ch	All	Tx7 Power MSB	Internally measured Tx power, channel 7	RO
77, 4Dh	All	Tx7 Power LSB		Opt.
78, 4Eh	All	Tx8 Power MSB	Internally measured Tx power, channel 8	RO
79, 4Fh	All	Tx8 Power LSB		Opt.

7.4.1.6 Control Fields

The control fields allow the host to dynamically change the behavior of the device. The changeable parameters include Tx input equalization, Rx pre-emphasis and Rx output amplitude in addition to disabling channels or squelching and setting the channel polarities. For each control, the host sets the code for what it wants and the device makes its best effort to provide the function indicated.

Table 23- Control Fields (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
80	7-4	Tx2 Equalization	Tx input equalization, channel 2	RW
50h	3-0	Tx1 Equalization	Tx input equalization, channel 1	Opt.
81	7-4	Tx4 Equalization	Tx input equalization, channel 4	RW
51h	3-0	Tx3 Equalization	Tx input equalization, channel 3	Opt.
82	7-4	Tx6 Equalization	Tx input equalization, channel 6	RW
52h	3-0	Tx5 Equalization	Tx input equalization, channel 5	Opt.
83	7-4	Tx8 Equalization	Tx input equalization, channel 8	RW
53h	3-0	Tx7 Equalization	Tx input equalization, channel 7	Opt.
84	7	Tx8 Disable	Tx channel disable, channel 8	RW
54h	6	Tx7 Disable	Tx channel disable, channel 7	Opt.
	5	Tx6 Disable	Tx channel disable, channel 6	for
	4	Tx5 Disable	Tx channel disable, channel 5	PC,AC,
	3	Tx4 Disable	Tx channel disable, channel 4	AO.
	2	Tx3 Disable	Tx channel disable, channel 3	R for
	1	Tx2 Disable	Tx channel disable, channel 2	SM
	0	Tx1 Disable	Tx channel disable, channel 1	
85	7	Tx8 Squelch Disable	Tx squelch disable, channel 8	RW
55h	6	Tx7 Squelch Disable	Tx squelch disable, channel 7	Opt.
	5	Tx6 Squelch Disable	Tx squelch disable, channel 6	
	4	Tx5 Squelch Disable	Tx squelch disable, channel 5	
	3	Tx4 Squelch Disable	Tx squelch disable, channel 4	
	2	Tx3 Squelch Disable	Tx squelch disable, channel 3	
	1	Tx2 Squelch Disable	Tx squelch disable, channel 2	
	0	Tx1 Squelch Disable	Tx squelch disable, channel 1	
86	7	Tx8 Force Squelch	Tx force squelch, channel 8	RW
56h	6	Tx7 Force Squelch	Tx force squelch, channel 7	Opt.
	5	Tx6 Force Squelch	Tx force squelch, channel 6	
	4	Tx5 Force Squelch	Tx force squelch, channel 5	
	3	Tx4 Force Squelch	Tx force squelch, channel 4	
	2	Tx3 Force Squelch	Tx force squelch, channel 3	
	1	Tx2 Force Squelch	Tx force squelch, channel 2	
	0	Tx1 Force Squelch	Tx force squelch, channel 1	
87	7	Tx8 Adaptive Equalization	Enable adaptive equalization Tx channel 8	RW
57h	6	Tx7 Adaptive Equalization	Enable adaptive equalization Tx channel 7	Opt.

	5	Tx6 Adaptive Equalization	Enable adaptive equalization Tx channel 6	
	4	Tx5 Adaptive Equalization	Enable adaptive equalization Tx channel 5	
	3	Tx4 Adaptive Equalization	Enable adaptive equalization Tx channel 4	
	2	Tx3 Adaptive Equalization	Enable adaptive equalization Tx channel 3	
	1	Tx2 Adaptive Equalization	Enable adaptive equalization Tx channel 2	
	0	Tx1 Adaptive Equalization	Enable adaptive equalization Tx channel 1	
88 58h	7	Tx8 CDR Enable	Tx CDR Enable, channel 8	RW Opt.
	6	Tx7 CDR Enable	Tx CDR Enable, channel 7	
	5	Tx6 CDR Enable	Tx CDR Enable, channel 6	
	4	Tx5 CDR Enable	Tx CDR Enable, channel 5	
	3	Tx4 CDR Enable	Tx CDR Enable, channel 4	
	2	Tx3 CDR Enable	Tx CDR Enable, channel 3	
	1	Tx2 CDR Enable	Tx CDR Enable, channel 2	
	0	Tx1 CDR Enable	Tx CDR Enable, channel 1	
89 59h	7	Rx8 CDR Enable	Rx CDR Enable, channel 8	RW Opt.
	6	Rx7 CDR Enable	Rx CDR Enable, channel 7	
	5	Rx6 CDR Enable	Rx CDR Enable, channel 6	
	4	Rx5 CDR Enable	Rx CDR Enable, channel 5	
	3	Rx4 CDR Enable	Rx CDR Enable, channel 4	
	2	Rx3 CDR Enable	Rx CDR Enable, channel 3	
	1	Rx2 CDR Enable	Rx CDR Enable, channel 2	
	0	Rx1 CDR Enable	Rx CDR Enable, channel 1	
90 5Ah	7	Rx8 Output Disable	Rx output disable, channel 8	RW Opt.
	6	Rx7 Output Disable	Rx output disable, channel 7	
	5	Rx6 Output Disable	Rx output disable, channel 6	
	4	Rx5 Output Disable	Rx output disable, channel 5	
	3	Rx4 Output Disable	Rx output disable, channel 4	
	2	Rx3 Output Disable	Rx output disable, channel 3	
	1	Rx2 Output Disable	Rx output disable, channel 2	
	0	Rx1 Output Disable	Rx output disable, channel 1	
91 5Bh	7	Rx8 Squelch Disable	Rx squelch disable, channel 8	RW
	6	Rx7 Squelch Disable	Rx squelch disable, channel 7	
	5	Rx6 Squelch Disable	Rx squelch disable, channel 6	
	4	Rx5 Squelch Disable	Rx squelch disable, channel 5	
	3	Rx4 Squelch Disable	Rx squelch disable, channel 4	
	2	Rx3 Squelch Disable	Rx squelch disable, channel 3	
	1	Rx2 Squelch Disable	Rx squelch disable, channel 2	
	0	Rx1 Squelch Disable	Rx squelch disable, channel 1	
92 5Ch	7	Channel 8 DataPathPwrUp	Enable Tx and Rx data path, channel 8	RW Opt.
	6	Channel 7 DataPathPwrUp	Enable Tx and Rx data path, channel 7	
	5	Channel 6 DataPathPwrUp	Enable Tx and Rx data path, channel 6	
	4	Channel 5 DataPathPwrUp	Enable Tx and Rx data path, channel 5	
	3	Channel 4 DataPathPwrUp	Enable Tx and Rx data path, channel 4	
	2	Channel 3 DataPathPwrUp	Enable Tx and Rx data path, channel 3	
	1	Channel 2 DataPathPwrUp	Enable Tx and Rx data path, channel 2	
	0	Channel 1 DataPathPwrUp	Enable Tx and Rx data path, channel 1	
93 5Dh	7-4	Reserved		RW Opt.
	3	Software Reset	Software reset, same effect as asserting the ResetL pin low and then high again	RW Opt.
	2-0	Vendor Specific		RW Opt.
94 5Eh	7-4	Rx2 Amplitude	Rx output amplitude, channel 2	RW Opt.
	3-0	Rx1 Amplitude	Rx output amplitude, channel 1	
95 5Fh	7-4	Rx4 Amplitude	Rx output amplitude, channel 4	RW Opt.
	3-0	Rx3 Amplitude	Rx output amplitude, channel 3	
96	7-4	Rx6 Amplitude	Rx output amplitude, channel 6	RW

60h	3-0	Rx5 Amplitude	Rx output amplitude, channel 5	Opt.
97	7-4	Rx8 Amplitude	Rx output amplitude, channel 8	RW
61h	3-0	Rx7 Amplitude	Rx output amplitude, channel 7	Opt.
98	7-4	Rx2 Pre-emphasis	Rx output pre-emphasis, channel 2	RW
62h	3-0	Rx1 Pre-emphasis	Rx output pre-emphasis, channel 1	Opt.
99	7-4	Rx4 Pre-emphasis	Rx output pre-emphasis channel 4	RW
63h	3-0	Rx3 Pre-emphasis	Rx output pre-emphasis, channel 3	Opt.
100	7-4	Rx6 Pre-emphasis	Rx output pre-emphasis, channel 6	RW
64h	3-0	Rx5 Pre-emphasis	Rx output pre-emphasis, channel 5	Opt.
101	7-4	Rx8 Pre-emphasis	Rx output pre-emphasis, channel 8	RW
65h	3-0	Rx7 Pre-emphasis	Rx output pre-emphasis, channel 7	Opt.

When a Tx output is disabled, it has negligible optical output power (Average power <-20dBm). When a Tx output is squelched and not disabled, it has a near-constant optical output with no high-speed variations that could be interpreted as valid data (OMA <-20dBm or per the relevant standard).

A DataPathPwrUp control bit becoming set turns on the electronics of the corresponding Tx data path, including the CDR (if any), but not the optical output; it also turns on the entire Rx data path so that incoming data can be received by the host.

Tx Input Equalization Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. The code values and the corresponding input equalization are defined as follows:

Table 24- Tx Input Equalization

Code Value	Bit pattern	Input Equalization
0	0000	No Equalization
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB
5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8	1000	8 dB
9	1001	9 dB
10	1010	10 dB
11	1011	11 dB
12	1100	12 dB
13	1101	Vendor Specific
14-15	111x	Vendor Specific

Rx Output Pre-emphasis Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. The code values and the corresponding output pre-emphasis are defined as follows:

Table 25- Rx Output Pre-emphasis

Code Value	Bit pattern	Output Pre-Emphasis
0	0000	No Pre-Emphasis
1	0001	1 dB
2	0010	2 dB
3	0011	3 dB
4	0100	4 dB

5	0101	5 dB
6	0110	6 dB
7	0111	7 dB
8-15	1xxx	Vendor Specific

Rx Output Amplitude Control has a four bit code block (bits 7-4 or 3-0) assigned to each channel. The code values and the corresponding output amplitude are defined as follows:

Table 26- Rx Output Amplitude

Code Value	Bit pattern	Output Amplitude
0	0000	100 mV (P-P)
1	0001	150 mV (P-P)
2	0010	200 mV (P-P)
3	0011	250 mV (P-P)
4	0100	300 mV (P-P)
5	0101	350 mV (P-P)
6	0110	400 mV (P-P)
7	0111	450 mV (P-P)
8	1000	500 mV (P-P)
9	1001	550 mV (P-P)
10	1010	600 mV (P-P)
11	1011	650 mV (P-P)
12	1100	700 mV (P-P)
13	1101	750 mV (P-P)
14	1110	800 mV (P-P)
15	1111	Vendor Specific

7.4.1.7 Interrupt Masks

The host system may control which flags result in an interrupt (IntL) by setting high individual bits from a set of masking bits in bytes 102-116. There is one masking bit per alarm or warning flag. A 1 value in a masking bit prevents the assertion of the hardware IntL pin by the corresponding latched flag bit. Masking bits are volatile and startup with all unmasked (masking bits 0).The mask bits may be used to prevent continued interruption from recurring conditions, which would otherwise continually reassert the hardware IntL pin (such as a monitor value hovering around an alarm or warning threshold value).

The clearing of an interrupt mask bit will cause an interrupt to be generated only if the corresponding interrupt flag became set while masked and has not been read (and cleared) by the host computer system. There is a maximum of one interrupt generated per occurrence of an alarm or warning condition.

Table 27- Interrupt Masks (Lower Page, active modules only)

Byte	Bits	Name	Description	Type
102 66h	7	M-Rx8 LOS	Masking bit for Rx LOS indicator, channel 8	RW C
	6	M-Rx7 LOS	Masking bit for Rx LOS indicator, channel 7	
	5	M-Rx6 LOS	Masking bit for Rx LOS indicator, channel 6	
	4	M-Rx5 LOS	Masking bit for Rx LOS indicator, channel 5	
	3	M-Rx4 LOS	Masking bit for Rx LOS indicator, channel 4	
	2	M-Rx3 LOS	Masking bit for Rx LOS indicator, channel 3	
	1	M-Rx2 LOS	Masking bit for Rx LOS indicator, channel 2	
	0	M-Rx1 LOS	Masking bit for Rx LOS indicator, channel 1	
103 67h	7	M-Tx8 LOS	Masking bit for Tx LOS indicator, channel 8	RW C
	6	M-Tx7 LOS	Masking bit for Tx LOS indicator, channel 7	

	5	M-Tx6 LOS	Masking bit for Tx LOS indicator, channel 6	
	4	M-Tx5 LOS	Masking bit for Tx LOS indicator, channel 5	
	3	M-Tx4 LOS	Masking bit for Tx LOS indicator, channel 4	
	2	M-Tx3 LOS	Masking bit for Tx LOS indicator, channel 3	
	1	M-Tx2 LOS	Masking bit for Tx LOS indicator, channel 2	
	0	M-Tx1 LOS	Masking bit for Tx LOS indicator, channel 1	
104 68h	7	M-Rx8 CDR LOL	Masking bit for RxCDR LOL indicator, channel 8	RW C
	6	M-Rx7 CDR LOL	Masking bit for RxCDR LOL indicator, channel 7	
	5	M-Rx6 CDR LOL	Masking bit for RxCDR LOL indicator, channel 6	
	4	M-Rx5 CDR LOL	Masking bit for RxCDR LOL indicator, channel 5	
	3	M-Rx4 CDR LOL	Masking bit for RxCDR LOL indicator, channel 4	
	2	M-Rx3 CDR LOL	Masking bit for RxCDR LOL indicator, channel 3	
	1	M-Rx2 CDR LOL	Masking bit for RxCDR LOL indicator, channel 2	
	0	M-Rx1 CDR LOL	Masking bit for RxCDR LOL indicator, channel 1	
105 69h	7	M-Tx8 CDR LOL	Masking bit for TxCDR LOL indicator, channel 8	RW C
	6	M-Tx7 CDR LOL	Masking bit for TxCDR LOL indicator, channel 7	
	5	M-Tx6 CDR LOL	Masking bit for TxCDR LOL indicator, channel 6	
	4	M-Tx5 CDR LOL	Masking bit for TxCDR LOL indicator, channel 5	
	3	M-Tx4 CDR LOL	Masking bit for TxCDR LOL indicator, channel 4	
	2	M-Tx3 CDR LOL	Masking bit for TxCDR LOL indicator, channel 3	
	1	M-Tx2 CDR LOL	Masking bit for TxCDR LOL indicator, channel 2	
	0	M-Tx1 CDR LOL	Masking bit for TxCDR LOL indicator, channel 1	
106 6Ah	7	M-Tx8Fault	Masking bit for TxFault indicator, channel 8	RW Opt
	6	M-Tx7Fault	Masking bit for TxFault indicator, channel 7	
	5	M-Tx6Fault	Masking bit for TxFault indicator, channel 6	
	4	M-Tx5Fault	Masking bit for TxFault indicator, channel 5	
	3	M-Tx4Fault	Masking bit for TxFault indicator, channel 4	
	2	M-Tx3Fault	Masking bit for TxFault indicator, channel 3	
	1	M-Tx2Fault	Masking bit for TxFault indicator, channel 2	
	0	M-Tx1Fault	Masking bit for TxFault indicator, channel 1	
107 6Bh	7	M-Temp High	Masking bit for first temperature monitor high alarm indicator	RW C
	6	M-Temp Low	Masking bit for first temperature monitor low alarm indicator	
	5	M-Temp High Warning	Masking bit for first temperature monitor high warning indicator	
	4	M-Temp Low Warning	Masking bit for first temperature monitor low warning indicator	
	3	M-Temp2 High	Masking bit for second temperature monitor high alarm indicator	
	2	M-Temp2 Low	Masking bit for second temperature monitor low alarm indicator	
	1	M-Temp2 High Warning	Masking bit for second temperature monitor high warning indicator	
	0	M-Temp2 Low Warning	Masking bit for second temperature monitor low warning indicator	
108 6Ch	7	M-Vcc3.3 High	Masking bit for 3.3 volts power supply monitor high alarm	RW C
	6	M-Vcc3.3 Low	Masking bit for 3.3 volts power supply monitor low alarm	
	5-4	Reserved		
	3	M-TEC Current High Alarm	Masking bit for TEC supply current monitor high alarm	
	2	M-TEC Current Fault	Masking bit for TEC supply current monitor fault alarm	
	1	M-Adapt-Complete	Masking bit for adaptation-complete flag	
	0	M-Init-Complete	Masking bit for initialization-complete flag	

1096Dh	7	M-Rx8 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 8	RWC
	6	M-Rx7 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 7	
	5	M-Rx6 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 6	
	4	M-Rx5 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 5	
	3	M-Rx4 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 4	
	2	M-Rx3 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 3	
	1	M-Rx2 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 2	
	0	M-Rx1 Power Low Warning	Masking bit for Rx input power low warning indicator, channel 1	
1106Eh	7	M-Rx8 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 8	RWC
	6	M-Rx7 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 7	
	5	M-Rx6 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 6	
	4	M-Rx5 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 5	
	3	M-Rx4 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 4	
	2	M-Rx3 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 3	
	1	M-Rx2 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 2	
	0	M-Rx1 Power Low Alarm	Masking bit for Rx input power low alarm indicator, channel 1	
1116Fh	7	M-Rx8 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 8	RWC
	6	M-Rx7 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 7	
	5	M-Rx6 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 6	
	4	M-Rx5 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 5	
	3	M-Rx4 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 4	
	2	M-Rx3 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 3	
	1	M-Rx2 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 2	
	0	M-Rx1 Power High Alarm	Masking bit for Rx input power high alarm indicator, channel 1	
11270h	7	M-Tx8 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 8	RWC
	6	M-Tx7 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 7	
	5	M-Tx6 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 6	
	4	M-Tx5 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 5	
	3	M-Tx4 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 4	

	2	M-Tx3 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 3	
	1	M-Tx2 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 2	
	0	M-Tx1 Bias Low Alarm	Masking bit for Tx bias current low alarm indicator, channel 1	
113 71h	7	M-Tx8 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 8	RW C
	6	M-Tx7 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 7	
	5	M-Tx6 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 6	
	4	M-Tx5 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 5	
	3	M-Tx4 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 4	
	2	M-Tx3 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 3	
	1	M-Tx2 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 2	
	0	M-Tx1 Bias High Alarm	Masking bit for Tx bias current high alarm indicator, channel 1	
114 72h	7	M-Tx8 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 8	RW C
	6	M-Tx7 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 7	
	5	M-Tx6 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 6	
	4	M-Tx5 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 5	
	3	M-Tx4 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 4	
	2	M-Tx3 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 3	
	1	M-Tx2 Power Low Alarm	Masking bit for Tx output power low alarm indicator, channel 2	
	0	M-Tx1 Power Low Alarm	Masking bit for TX output power low alarm indicator, channel 1	
115 73h	7	M-Tx8 Power High Alarm	Masking bit for TX output power high alarm indicator, channel 8	RW C
	6	M-Tx7 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 7	
	5	M-Tx6 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 6	
	4	M-Tx5 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 5	
	3	M-Tx4 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 4	
	2	M-Tx3 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 3	
	1	M-Tx2 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 2	
	0	M-Tx1 Power High Alarm	Masking bit for Tx output power high alarm indicator, channel 1	
116 74h	All	Reserved	(PAM4 / WDM Alarm Masks)	
117-118	All	Vendor Specific		

7.4.1.8 Password Entry and Change

Bytes 119-126 are reserved for the password entry function. The Password entry bytes may be write only and will be retained until power down, reset, or rewritten by host. This function is used to control write access to vendor specific page 02h (eeprom) and other upper pages. Additionally, module vendors may use this function to implement write protection of Serial ID and other read only information. Note that multiple module manufacturer passwords may be defined to allow selective access to write to various sections of memory.

7.4.1.9 Page Select Byte

The value written to the page select determines which upper page is accessed at addresses 128 to 255 (80h to FFh). Attempting to access non-existent upper pages will cause writes to be ignored and reads to return all zeros, all ones, or some other preset value.

7.4.2 Upper Page 00h

Upper Page 00h consists of the Serial ID and is used for read only identification information. The Serial ID is divided into the Base ID Fields, Extended ID Fields and Vendor Specific ID Fields. The format of the Serial ID Memory Map is illustrated as follows:

Table 28- Upper Page 0 Overview (Page 00h)

Address	Size (bytes)	Name	Description
Base ID Fields:			
128	1	Identifier	Identifier Type of module
129	1	Ext. Identifier	Extended Identifier
130	1	Connector Type	Code for media connector type
131-138	8	Specification compliance	Code for electronic compatibility or optical compatibility
139	1	Encoding	Code for serial encoding algorithm
140	1	BR, nominal	Nominal bit rate, units of 100 MBits/s
141	1	Extended rate select compliance	Tags for extended rate select compliance
142-146	5	Link length	Link length / transmission media
147	1	Device technology	Device technology
148-163	16	Vendor name	Vendor name (ASCII)
164	1	Extended Module	Extended Module codes for InfiniBand
165-167	3	Vendor OUI	Vendor IEEE company ID
168-183	16	Vendor PN	Part number provided by vendor (ASCII)
184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
186-187	2	Wavelength or Copper	Nominal laser wavelength

		cable Attenuation	(wavelength=value/20 in nm) or copper cable attenuation in dB at 2.5GHz (Adrs 186) and 5.0GHz (Adrs 187)
188-189	2	Wavelength tolerance	Guaranteed range of laser wavelength(+/- value) from nominal wavelength.(wavelength Tolerance=value/200 in nm)
190	1	Max case temp.	Maximum case temperature in degrees C
191	1	CC_BASE	Check code for base ID fields (addresses 128-190 inclusive)
Extended ID Fields:			
192-195	4	Options	Indicates which optional capabilities are implemented in the module
196-211	16	Vendor S/N	Vendor product serial number
212-219	8	Date Code	Vendor’s manufacturing date code
220	1	Diagnostic Monitoring Type	Indicates which types of diagnostic monitoring are implemented in the module
221-222	2	Enhanced Options	Indicates which optional enhanced features are implemented in the module.
223	1	CC_EXT	Check code for the Extended ID Fields (addresses 192-222 inclusive)
224-238	15	Device Properties	Provides detailed information about the device
239	1	CC-PROP	Check code for the Device Properties Fields (addresses 224-2382 inclusive)
Vendor Specific ID Fields:			
240-255	16	Vendor-Specific	Vendor-specific ID information

7.4.2.1 Identifier and Extended Identifier

The identifier value specifies the physical device described by the serial information. This field should contain the same value as byte 0 in the lower page. These values are maintained in the Transceiver Management section of SFF-8024.

The extended identifier identifies the power consumption class that the device belongs to and provides additional information such as whether the module card contains a CDR function. The power classes indicate the power consumed per circuit board.

Table 29- Identifiers (Page 00h)

Byte	Bits	Name	Description	Type
128 80h	All	Identifier	Identifier - Type of Serial Module - See SFF-8024. A value of 18h indicates a QSFP-DD transceiver.	RO Rqrd.
129 81h	7-5	Module Card Power Class	000: Power class 1 (1.5 W maximum) 001: Power class 2 (3.5 W maximum) 010: Power class 3 (5.0 W maximum) 011: Power class 4 (7.0 W maximum) 100: Power class 5 (10.0 W maximum) 101: Power class 6 (12.0 W maximum) 110: Power class 7 (14.0 W maximum) 111: Power class 8 (>14 W maximum – see byte 229)	RO Rqrd.
	4	CLEI code presence	Coded 1 if CLEI code present in page 02h, otherwise coded 0	

	3	CDR present in TX	Coded 1 if Tx channels include CDRs	
	2	CDR present in RX	Coded 1 if Rx channels include CDRs	
	1	MDIO supported	Coded 1 if MDIO serial interface implemented	
	0	Max two-wire serial speed	0: Serial interface speed 0-400 KHz 1: Serial interface speed 0-1 MHz	

7.4.2.2 Connector Type

The Connector Type entry at Page 00H Byte 130 indicates the connector type for the separable portion of the free side device when the device has detachable media. These values are maintained in the Transceiver Management section of SFF-8024.

7.4.2.3 Specification Compliance

The Specification Compliance fields are bit-significant indicators defining the electronic or optical interfaces that are supported by the device. For Fibre Channel support, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated. The definition of each bit in these fields is maintained in the Serial ID section of SFF-8636.

Table 30- Specification compliance (Page 00h)

Byte	Bits	Name	Description	Type
131 83h	7-2	Reserved		RO Rqrd.
	1	100GBASE-CR4	802.3bj Section 92	
	0	CAUI-4	802.3bm Annex 83E	
132 84h	7-4	Reserved		RO Rqrd.
	3	LAUI-2 C2M	802.3cd Annex 135D	
	2	50GAUI-2 C2M	802.3cd Annex 135E	
	1	50GAUI-1 C2M	802.3cd Annex 135G	
	0	CDAUI-8 C2M	802.3bs Annex 120E	
133- 138	All	Reserved		RO Rqrd.

7.4.2.4 Encoding

The encoding value indicates the serial encoding mechanism that is the nominal design target of the particular device. These values are maintained in the Transceiver Management section of SFF-8024.

7.4.2.5 Nominal Bit Rate

The nominal bit rate (BR, nominal) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. The actual information transfer rate may depend on the encoding of the data, as defined by the encoding value. A value of 0 indicates that the bit rate is defined elsewhere (see below).

7.4.2.6 Extended Rate Select and Configuration

The Extended Rate Select Compliance field is used to allow a single device the flexibility to comply with single or multiple Extended Rate Select definitions.

Table 31- Extended Rate Select compliance (Page 00h)

Byte	Bits	Name	Description	Type
141 8Dh	7-2		Reserved	RO Rqrd.
	1	Rate Select Version 2	Coded 1 if QSFP+ Rate Select Version 2 implemented. This functionality is different from SFF-8472 and SFF-8431.	
	0	Rate Select Version 1	Coded 1 if QSFP+ Rate Select Version 1 implemented. This functionality is different from SFF-8472 and SFF-8431.	

7.4.2.7 Link Length

The link length fields specify the data link length in various transmission media. In each case, a value of zero means that the device does not support the transmission media or that the length information must be determined from the device technology.

Table 32- Link Length (Page 00h)

Address	Bits	Name	Description	Type
142 8Eh	All	Length (SMF)	Link length supported for SMF fiber in km	RO Rqrd.
143 8Fh	All	Length (OM3 50 um)	Link length supported for EBW 50/125 µm fiber (OM3), units of 2m	RO Rqrd.
144 90h	All	Length (OM2 50 um)	Link length supported for 50/125 µm fiber (OM2), units of 1m	RO Rqrd.
145 91h	All	Length (OM1 62.5 um)	Link length supported for 62.5/125 µm fiber (OM1), units of 1m	RO Rqrd.
146 92h	All	Length (Copper or active cable)	Link length of copper or active cable, units of 1 m	RO Rqrd.

The link length supported for SMF fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using single mode fiber. The supported link length is as specified in the SFF 8074i standard. The value is in units of kilometers.

The link length supported for OM3 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 2000 MHZ*km (850 nm) extended bandwidth 50 micron core multimode fiber. The value is in units of two meters.

The link length supported for OM2 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 500 MHz*km (850 nm and 1310 nm) 50 micron multi-mode fiber. The value is in units of one meter.

The link length supported for OM1 fiber specifies the link length that is supported by the device while operating in compliance with the applicable standards using 200 MHz*km (850 nm) and 500 MHz*km (1310 nm) 62.5 micron multi-mode fiber. The value is in units of one meter.

The link length for copper or active cable specifies the link length of the cable assembly. The value is in units of one meter. Link lengths less than 1 meter shall indicate 1 meter. A value of zero means that the device is not a cable assembly or that the length information must be determined from the device technology. A value of 255 means that the device supports a link length greater than 254 m.

7.4.2.8 Device Technology

The device technology byte specifies the technology used in the device. Four bits are used to identify the technology type and the remaining four bits are used to indicate options implemented.

Table 33- Device technology (Page 00h)

Byte	Bits	Name	Description	Type
147 93h	7-4	Technology	Transmitter technology code	RO Rqrd.
	3	Wavelength control	0: No wavelength control 1: Active wavelength control	
	2	Cooling	0: Uncooled transmitter device 1: Cooled transmitter	
	1	Detector type	0: PIN detector 1: APD detector	
	0	Tunable	0: Transmitter not tunable 1: Transmitter tunable	

Table 34- Technology values

Code	Description of physical device
00h	850 nm VCSEL
01h	1310 nm VCSEL
02h	1550 nm VCSEL
03h	1310 nm FP
04h	1310 nm DFB
05h	1550 nm DFB
06h	1310 nm EML
07h	1550 nm EML
08h	Others
09h	1490 nm DFB
0Ah	Copper cable unequalized
0Bh	Copper cable passive equalized
0Ch	Copper cable, near and far end limiting active equalizers
0Dh	Copper cable, far end limiting active equalizers
0Eh	Copper cable, near end limiting active equalizers
0Fh	Copper cable, linear active equalizers

7.4.2.9 Vendor Name

The vendor name is a 16 character field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

7.4.2.10 Extended Module Codes

The Extended Module Code defines the electronic or optical interfaces for InfiniBand that are supported by the device.

Table 35- Extended module code (Page 00h)

Byte	Bits	Name	Description	Type
164 A4h	7-6	Reserved		RO Rqrd.
	5	LDR Speed	Coded 1 for LDR Speed support	
	4	EDR Speed	Coded 1 for EDR Speed support	
	3	FDR Speed	Coded 1 for FDR Speed support	
	2	QDR Speed	Coded 1 for QDR Speed support	
	1	DDR Speed	Coded 1 for DDR Speed support	
	0	SDR Speed	Coded 1 for SDR Speed support	

7.4.2.11 Vendor Organizationally Unique Identifier

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

7.4.2.12 Vendor Part Number

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor part number is unspecified.

7.4.2.13 Vendor Revision Number

The vendor revision number (vendor rev) is a 2-byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor’s product revision number. A value of all zero in the field indicates that the vendor Rev is unspecified.

7.4.2.14 Wavelength or Copper Cable Attenuation

The wavelength field specifies the nominal transmitter output wavelength at room temperature; this is a16-bit value with byte 186 as the high order byte and byte 187 as the low order byte. The laser wavelength value is equal to the 16-bit integer value of the wavelength in nm divided by 20 (units of 0.05nm). This resolution should be adequate to cover all relevant wavelengths yet provide enough resolution for all expected applications. For accurate representation of controlled wavelength applications, this value should represent the center of the guaranteed wavelength range.

If the cable is identified as a copper cable, these addresses will be used to define the cable attenuation. Address 186 (00-FFh) holds an 8 bit value indicating the copper cable attenuation at 7 GHz in units of 1 dB. Address 187 (00-FFh) holds an 8 bit value indicating the copper cable attenuation at 12.9 GHz in units of 1 dB. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.

7.4.2.15 Wavelength Tolerance or Copper Cable Attenuation

The wavelength tolerance is the guaranteed +/- range of the transmitter output wavelength under all normal operating conditions; this is a 16-bit value with byte 188 as the high order byte and byte 189 as the low order byte. The laser wavelength tolerance is equal to the 16-bit integer value in nm divided by 200 (units of 0.005nm). Thus, the following two examples:

Example 1:
10GBASE-LR Wavelength Range = 1260 to 1355 nm
Nominal Wavelength in bytes 186 - 187 = 1307.5 nm.
Represented as INT (1307.5 nm * 20) = 26150 = 6626h
Wavelength Tolerance in bytes 188 - 189 = 47.5nm.
Represented as INT (47.5 nm * 200) = 9500 = 251Ch

Example 2:
ITU-T Grid Wavelength = 1534.25 nm with 0.236 nm Tolerance
Nominal Wavelength in bytes 186 - 187 = 1534.25 nm.
Represented as INT (1534.25nm * 20) = 30685 = 77DDh
Wavelength Tolerance in bytes 188 - 189 = 0.236 nm.
Represented as INT (0.236 nm * 200) = 47 = 002Fh

If the module is identified as copper cable these registers will be used to define the cable attenuation. An indication of 0 dB attenuation refers to the case where the attenuation is not known or is unavailable.
Byte 188 (00-FFh) is the copper cable attenuation at 7.0 GHz in units of 1 dB.
Byte 189 (00-FFh) is the copper cable attenuation at 12.9 GHz in units of 1 dB.

7.4.2.16 Maximum Case Temperature

The maximum case temperature field allows specification of a maximum case temperature other than the standard default of 70C. The maximum case temperature is an 8-bit value in degrees C.

7.4.2.17 CC-BASE

The check code is a one byte code that can be used to verify that the first 63 bytes of serial information in the device is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 128 to byte 190, inclusive.

7.4.2.18 Options

The bits in the options field shall specify the options implemented in the module.

Table 36- Options (Page 00h)

Byte	Bit	Name	Description	Type
192 C0h	All	Extended Ethernet Compliance Codes	Compliance codes as defined in SFF-8024 Table 4-4	RO Rqrd.
193 C1h	7	Rx Squelch present	Coded 1 if Rx Squelch provided	RO Rqrd.
	6	Rx Loss of Signal implemented	Coded 1 if Rx LOS alarm flags provided	
	5	Rx polarity flip implemented	Coded 1 if Rx polarity flip control provided	
	4	Tx polarity flip implemented	Coded 1 if Tx polarity flip control provided	
	3	Tx adaptive Equalization implemented	TX Input Equalization Auto Adaptive Capable, coded 1 if implemented, else 0.	
	2	TX input Equalization implemented	Coded 1 if Tx equalization control provided	
	1	Rx pre-emphasis implemented	Coded 1 if Rx pre-emphasis control provided	
	0	Rx output amplitude implemented	Coded 1 if Rx output amplitude control provided	
194 C2h	7	Tx CDR On/Off Control implemented	Coded 1 if Tx CDR control provided	RO Rqrd.
	6	Rx CDR On/Off Control implemented	Coded 1 if Rx CDR control provided	
	5	Tx CDR Loss of Lock (LOL) Flag implemented	Coded 1 if Tx CDR LOL alarm flag provided	
	4	Rx CDR Loss of Lock (LOL) Flag implemented	Coded 1 if Rx CDR LOL alarm flag provided	
	3	Rx Squelch Disable implemented	Coded 1 if Rx Squelch Disable control provided	
	2	Rx Output Disable implemented	Coded 1 if Rx Output Disable control provided	
	1	Tx Squelch Disable implemented	Coded 1 if Tx Squelch Disable control provided	
	0	Tx Squelch present	Coded 1 if Tx Squelch provided	
195 C3h	7	Memory page 02 present	Coded 1 if memory page 02h provided	RO Rqrd.
	6	Memory page 01 present	Coded 1 if memory page 01h provided	
	5	Tx Rate Select implemented	Coded 1 if Tx Rate Select control provided	
	4	Tx Disable implemented	Coded 1 if Tx Disable control provided	
	3	Tx Fault Flag implemented	Coded 1 if Tx Fault supported	
	2	Tx Squelch Pave	Coded 1 if Tx Squelch implemented to reduce Pave; coded 0 if Tx Squelch implemented to reduce OMA	
	1	Tx LOS Flag implemented	Coded 1 if Tx LOS alarm flag provided	
	0	Reserved		

7.4.2.19 Vendor Serial Number

The vendor serial number (vendor SN) is a 16-character field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor’s serial number for the Product. A value of all zero in the 16-byte field indicates that the vendor part number is unspecified.

7.4.2.20 Date Code

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the following format:

```
Bytes 212-213:    ASCII code, two low order digits of year (00=2000)
Bytes 214-215:    ASCII code digits of month (01=Jan through 12=Dec)
Bytes 216-217:    ASCII code day of month (01-31)
Bytes 218-219:    ASCII code, vendor specific lot code, may be blank
```

7.4.2.21 Diagnostic Monitoring Type

Diagnostic Monitoring Type is a 1-byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular module. Bit indicators are as follows:

Table 37- Diagnostic Monitoring Type (Page 00h)

Byte	Bit	Name	Description	Type
220 DCh	7-5	Reserved		RO Rqrd.
	4	Rx Optical Power Monitor implemented	Coded 1 if individual Rx Power Monitors provided	
	3	Rx Optical Power Measurement Type	Rx Power measurement type, 0=OMA, 1=average power	
	2	Tx Optical Power Channel Monitoring implemented	Coded 1 if individual Tx Optical Power Monitors provided	
	1	Tx Bias Monitor implemented	Coded 1 if individual Tx Bias Monitors provided	
	0	Reserved		

7.4.2.22 Enhanced Options

The bits in the enhanced options field specify the enhanced options implemented in the module.

Table 38- Enhanced Options (Page 00h)

Byte	Bit	Name	Description	Type
221 DDh	7	User defined		RO Rqrd.
	6	Vendor Specific		
	5	Internal 3.3 volts Monitor implemented	Coded 1 if Internal 3.3 volts Vcc Monitor provided	
	4	Power change complete flag implemented	Coded 1 if Initialization Complete flag set on completion of a power state change	
	3	Rx Rate Select implemented	Coded 1 if Rx Rate Select control provided	
	2	Application Select implemented	Coded 1 if Application Select control provided	
	1-0	Reserved		
222 DEh	All	Extended Bit Rate		RO Rqrd.

To permit bit rates in excess of 25.4 Gbps, an extended bit rate field has been added in Byte 222 to supplement the existing values in Byte 140. The legacy Byte 140 contains bit rate at 100 Mbps, which is limited to 25.4 Gbps. The new Byte 222 contains bit rate at 250 Mbps, enabling up to 63.5 Gbps. A value of zero means this field is unspecified.

7.4.2.23 CC-EXT

The check code is a one-byte code that can be used to verify that the first 31 bytes of extended serial information in the module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 192 to byte 222, inclusive.

7.4.2.24 Device Properties

The device properties area provides detailed information about the device.

The global options bits define whether or not channels can be controlled individually or are ganged together.

Table 39- Device Properties (Page 00h)

Byte	Bit	Name	Description	Type
224, E0h	All	Propagation Delay MSB	Propagation delay of the non-separable AOC in multiples of 10ns rounded to the nearest 10 ns.	RO Opt.
225, E1h	All	Propagation Delay LSB		
226, E2h	All	PCI Express MSB	See relevant PCI-SIG documents	RO Opt.
227, E3h	All	PCI Express LSB		
228, E4h	All	Min Operating Voltage	Minimum voltage which the device can operate at in multiples of 20 mV, rounded up to the next whole multiple of 20 mV	RO Opt.
229, E5h	All	Max Power	Maximum power consumption in multiples of 0.1 W rounded up to the next whole multiple of 0.1 W	RO Opt.
230, E6h	All	Max CDR Power	Incremental maximum power consumption per CDR per channel in multiples of 0.01 W rounded up to the next whole multiple of 0.01 W	RO Opt.
231, E7h	7-5	ModSelL wait time exponent	The ModSelL wait time value is the mantissa x 2^exponent expressed in micro-seconds. In other words, the mantissa field is shifted up by the number of bits indicated in the exponent field (time = mantissa << exponent)	RO Opt.
	4-0	ModSelL wait time mantissa		
232, E8h	7	Global Tx Disable	Coded 1 if any Tx Disable control bit being set disables all Tx channels	RO Opt.
	6	Global Tx Squelch Disable	Coded 1 if any Tx Squelch Disable control bit being set disables squelching for all Tx channels	
	5	Global Tx Equalization	Coded 1 if writing to any Tx Equalization control field writes the same value to all Tx Equalization control fields	
	4	Global Rx Output Disable	Coded 1 if any Rx Output Disable control bit being set disables the output on all Rx channels	
	3	Global Rx Squelch Disable	Coded 1 if any Rx Squelch Disable control bit being set disables squelching for all Rx channels	
	2	Global Rx Pre-Emphasis	Coded 1 if writing to any Rx Pre-Emphasis control field writes the same	

			value to all Rx Pre-Emphasis control fields	
	1	Global Rx Output Amplitude	Coded 1 if writing to any Rx Output Amplitude control field writes the same value to all Rx Output Amplitude control fields	
	0	Reserved		
233, E9h	7-4	Max Rx Output Amplitude	Maximum value of the Rx Output Amplitude control supported	RO Opt.
	3-0	Max Rx Pre-Emphasis	Maximum value of the Rx Pre-Emphasis control supported	
234, EAh	7-4	Max Tx Equalization	Maximum value of the Tx Equalization control supported	RO Opt.
	3-0	Reserved		
235, EBh	7-4	Max TX DataPathDeinit Duration	Encoded maximum duration of the DataPathDeinit transient state during module initialization. Measured from rising edge of stop condition of 2 wire serial write of datapathpwr bit. See Table 40	RO Opt.
	3-0	Max DataPathInit Duration	Encoded maximum duration of the transient DataPathInit state during module initialization. See Table 40	
236, ECh	All	Reserved		
237, EDh	All	Reserved		
238, EEh	All	Reserved		
239, EFh	All	CC-PROP	Check code for property ID fields (Bytes 224-238)	RO R.

7.4.2.25 ModSelL Wait Time

This field defines the required setup time for the ModSelL signal after the host asserts a low level on ModSelL before the start of a two-wire serial bus transaction, and the required delay from completion of a two-wire serial bus transaction before the host can de-assert the ModSelL signal. For example, if the module wait time is 1.6ms, the mantissa field (bits 4-0) will be 11001b and the exponent field (bits 7-5) will be 110b indicating six zeros after the 11001b for a net result of 11001000000b or 1600 decimal.

7.4.2.26 Transient State Durations

The Max DataPathInit Duration and Max DataPathReady Duration fields are used to allow the module to inform the host of the maximum duration of transient states. (Figure 40 Initialization State Machine) Note that the module may interrupt the host at any time before the maximum duration reported, to report that the state is complete. The following table defines the encodings used for both fields.

Table 40- State Duration Encoding

Encoding	Maximum State Duration
0000b	Maximum state duration is less than 1 ms
0001b	1 ms <= maximum state duration < 5 ms
0010b	5 ms <= maximum state duration < 10 ms
0011b	10 ms <= maximum state duration < 50 ms
0100b	50 ms <= maximum state duration < 100 ms
0101b	100 ms <= maximum state duration < 500 ms
0110b	500 ms <= maximum state duration < 1 s
0111b	1 s <= maximum state duration < 5 s
1000b	5 s <= maximum state duration < 10 s
1001b	10 s <= maximum state duration < 1 min
1010b	1 min <= maximum state duration < 5 min
1011b	5 min <= maximum state duration < 10 min
1100b	10 min <= maximum state duration < 50 min
1101b	Maximum state duration >= 50 min
1110b	Reserved
1111b	Reserved

7.4.2.27 CC-PROP

The check code is a one-byte code that can be used to verify that the first 15 bytes of device property information in the module is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 224 to byte 238, inclusive.

7.4.2.28 Vendor-Specific ID

The vendor-specific ID area (bytes 240 to 255) may be used to provide any additional ID information required by the customers.

7.4.3 Upper Page 01h

The presence of upper page 01h is conditional on the state of bit 2 in Page 0h byte 195 Table 36. Bytes 188-215 are user defined. The format of the page is as defined in SFF-8079. The page has a two-byte header followed by up to 63 two-byte entries. The header is illustrated as follows:

Table 41- Application Table Header (Page 01h, active modules only)

Byte	Bits	Name	Description	Type
128 80h	7-0	CC-APPS	Check code for the Application Select Table. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 129 to byte 255, inclusive	RO Opt.
129 81h	7	Reserved		RO Opt.
	6	Reserved		
	5-0	AST Table Length TL	Specifies the number of entries used in the table; TL is valid between value 0 (one entry) and 63 (63 entries)	

In the legacy AST table format, the two-byte entries have a category identifier in the first byte and a variant identifier in the second byte. Categories 0 to 20h (legacy categories) are defined in SFF-8089 along with all their variants.

Table 42- Legacy Table Entry (Page 01h, active modules only)

Byte	Bits	Name	Description	Type
130+ 2*TL	7	Must be zero	Legacy format indicator	RO Opt.
	6-5	Reserved		
	4-0	Category	Application type (e.g. InfiniBand)	
131+ 2*TL	All	Variant	Variant within the application type	RO Opt.

The extended format table entries are indicated by the high order bit of the first byte being set to one. The remaining 15 bits of the byte pair form a single 15-bit integer indicating the data rate in multiples of 5 Mb/s rounded to the nearest 5 Mb/s.

Table 43- Extended Table Entry (Page 01h, active modules only)

Byte	Bits	Name	Description	Type
130+ 2*TL	7	Must be one	Extended format indicator	RO Opt.
	6-5	Data Rate MSB	High order bits of data rate in multiples of 5 Mb/s	
131+ 2*TL	All	Data Rate LSB	Low order byte of data rate in multiples of 5 Mb/s	RO Opt.

7.4.4 Upper Page 02h

Upper Page 02h is optionally provided as user writable EEPROM. The host system may read or write this memory for any purpose. If bit 4 of Page 0h byte 129 is set, the first 10 bytes of upper page 02h (bytes 128 to 137) will be used to store the CLEI code for the device. To prevent unintentional changes, upper page 02h may be password protected.

7.4.5 Upper Page 03h

The upper memory map page 03h contains module thresholds, channel thresholds, and optional channel controls. Upper page 03h is subdivided into several areas as illustrated in the following table:

Table 44- Upper Page 3 Overview (Page 03h)

Address	Description	Type
128 – 175	Module Thresholds (48 Bytes)	Read-only
176 – 223	Channel Thresholds (48 Bytes)	Read-only
224 – 251	Extended Channel Controls (28 bytes)	Read/Write
252 – 255	Hardware/Firmware ID (4 bytes)	Read-only

7.4.5.1 Module Thresholds

Each quantitative module monitor has a corresponding high alarm and low alarm threshold. Some monitors may also have high warning and low warning thresholds. For each monitor that is implemented, high and low alarm thresholds are required. These factory-preset values allow the user to determine when a particular value is outside of normal limits as determined by the device manufacturer. The values are stored in the same format as the corresponding monitor value reported in lower page 00h. The threshold values are stored in read-only memory in upper memory page 03h as shown below:

Table 45- Module Thresholds (Page 03h, active modules only)

Address	Description	Type
128 – 129	High alarm threshold for first temperature monitor	RO C
130 – 131	Low alarm threshold for first temperature monitor	RO C
132 – 133	High warning threshold for first temperature monitor	RO Opt.
134 – 135	Low warning threshold for first temperature monitor	RO Opt.
136 – 137	High alarm threshold for second temperature monitor (if any)	RO Opt.
138 – 139	Low alarm threshold for second temperature monitor (if any)	RO Opt.
140 – 141	High warning threshold for second temperature monitor (if any)	RO Opt.
142 – 143	Low warning threshold for second temperature monitor (if any)	RO Opt.
144 – 145	High alarm threshold for 3.3 volt power supply monitor	RO C
146 – 147	Low alarm threshold for 3.3 volt power supply monitor	RO C
148 – 149	Reserved - High warning threshold for 3.3 volt power supply monitor	RO
150 – 151	Reserved - Low warning threshold for 3.3 volt power supply monitor	RO
152 – 153	Reserved - High alarm threshold for TEC supply current (if any)	RO C
154 – 155	Reserved - Low alarm threshold for TEC supply current (if any)	RO C
156 – 157	Reserved	RO
158 – 159	Reserved	RO
160 – 161	Reserved	RO Opt.
162 – 163	Bit rate for extended rate select code 001 in multiples of 5 Mbps rounded to the nearest 5 Mbps	RO Opt.
164 – 165	Bit rate for extended rate select code 010	RO
166 – 167	Bit rate for extended rate select code 011	RO
168 – 169	Bit rate for extended rate select code 100	RO
170 – 171	Bit rate for extended rate select code 101	
172 – 173	Bit rate for extended rate select code 110	
174 – 175	Bit rate for extended rate select code 111	

7.4.5.2 Channel Thresholds

Each quantitative channel monitor also has a corresponding high alarm and low alarm threshold. Some monitors may also have high warning and low warning thresholds. These threshold values are stored in read-only memory in upper memory page 03h as shown below:

Table 46- Channel Thresholds (Page 03h, active modules only)

Address	Description	Type
176 – 177	High alarm threshold for Rx optical power monitor	RO C
178 – 179	Low alarm threshold for Rx optical power monitor	RO C
180 – 181	Reserved - High warning threshold for Rx optical power monitor	RO
182 – 183	Low warning threshold for Rx optical power monitor	RO Opt.
184 – 185	High alarm threshold for Tx bias current monitor	RO C
186 – 187	Low alarm threshold for Tx bias current monitor	RO C
188 – 189	Reserved - High warning threshold for Tx bias current monitor	RO
190 – 191	Reserved - Low warning threshold for Tx bias current monitor	RO
192 – 193	High alarm threshold for Tx optical power monitor (if any)	RO C
194 – 195	Low alarm threshold for Tx optical power monitor (if any)	RO C
196 – 197	Reserved - High warning threshold for Tx optical power monitor (if any)	RO
198 – 199	Reserved - Low warning threshold for Tx optical power monitor (if any)	RO
200 – 201	Reserved	RO Opt.
202 – 203	Reserved	RO Opt.
204 – 205	Reserved	RO Opt.
206 – 207	Reserved	RO Opt.
208 – 209	Reserved	RO Opt.
210 – 211	Reserved	RO Opt.
212 – 213	Reserved	RO Opt.
214 – 223	Reserved	RO

7.4.5.3 Extended Channel Controls

The extended channel control fields allow the host computer system to change the gross behavior of the device. The changeable parameters include data rate and application supported by the channel.

Rate Select is an optional control used to limit the receiver bandwidth for compatibility with multiple data rates and allows the transmitter to be fine-tuned for specific data rates. The module may:

a) Provide no support for rate selection
b) Rate selection using extended rate select
c) Rate selection with application select tables

The Extended Rate Select Controls have a three bit code block assigned to each channel. Code 000b indicates no data rate selection. Code 001b to code 111b call for the data rate indicated in Table 45; a value of zero in a particular table entry indicates that there is no optimization available for that control code.

When the Rate Select declaration bits (Page 0h, byte 221, bits 2 and 3) have the values 1 and 0 respectively, the Application Select method defined in Page 01h may be used. The host reads the entire Application Select Table (AST) in page 01h to determine the capabilities of the module card. The host controls each channel separately by writing a Control Mode and Table Select (TS) byte to the Application Select bytes. The two-bit Control Mode value occupies the most-significant bits of the control byte and defines the application control mode; a value of zero indicates that the extended rate select method should be used whereas a non-zero value indicates that the AST table in Page 01h should be used. For the AST table mode, the six-bit Table Select value occupies the least-significant bits of the control byte and selects module card behavior from the Application Select Table among the 63 possibilities described there (values 000000b to 111110b). Note that value 111111b is invalid. For the Extended Rate Select mode (0) the three-bit code value occupies the least significant bits of the control byte.

The extended channel controls in upper page 03h are as follows:

Table 47- Extended Channel Controls (Page 03h, active modules only)

Byte	Bits	Name	Description	Type
224	7-6	Tx1 AST Control Mode	Tx application select, channel 1	RW
E0h	5-0	Tx1 AST Select Index (Mode 2)		Opt.
	2-0	Tx1 Rate Select (Mode 0)	Tx data rate select, channel 1	
225	7-6	Tx2 AST Control Mode	Tx application select, channel 2	RW
E1h	5-0	Tx2 AST Select Index (Mode 2)		Opt.
	2-0	Tx2 Rate Select (Mode 0)	Tx data rate select, channel 2	
226	7-6	Tx3 AST Control Mode	Tx application select, channel 3	RW
E2h	5-0	Tx3 AST Select Index (Mode 2)		Opt.
	2-0	Tx3 Rate Select (Mode 0)	Tx data rate select, channel 3	
227	7-6	Tx4 AST Control Mode	Tx application select, channel 4	RW
E3h	5-0	Tx4 AST Select Index (Mode 2)		Opt.
	2-0	Tx4 Rate Select (Mode 0)	Tx data rate select, channel 4	
228	7-6	Tx5 AST Control Mode	Tx application select, channel 5	RW
E4h	5-0	Tx5 AST Select Index (Mode 2)		Opt.
	2-0	Tx5 Rate Select (Mode 0)	Tx data rate select, channel 5	
229	7-6	Tx6 AST Control Mode	Tx application select, channel 6	RW
E5h	5-0	Tx6 AST Select Index (Mode 2)		Opt.
	2-0	Tx6 Rate Select (Mode 0)	Tx data rate select, channel 6	
230	7-6	Tx7 AST Control Mode	Tx application select, channel 7	RW
E6h	5-0	Tx7 AST Select Index (Mode 2)		Opt.
	2-0	Tx7 Rate Select (Mode 0)	Tx data rate select, channel 7	
231	7-6	Tx8 AST Control Mode	Tx application select, channel 8	RW
E7h	5-0	Tx8 AST Select Index (Mode 2)		Opt.
	2-0	Tx8 Rate Select (Mode 0)	Tx data rate select, channel 8	
232	7-6	Rx1 AST Control Mode	Rx application select, channel 1	RW
E8h	5-0	Rx1 AST Select Index (Mode 2)		Opt.
	2-0	Rx1 Rate Select (Mode 0)	Rx data rate select, channel 1	
233	7-6	Rx2 AST Control Mode	Rx application select, channel 2	RW
E9h	5-0	Rx2 AST Select Index (Mode 2)		Opt.
	2-0	Rx2 Rate Select (Mode 0)	Rx data rate select, channel 2	
234	7-6	Rx3 AST Control Mode	Rx application select, channel 3	RW
EAh	5-0	Rx3 AST Select Index (Mode 2)		Opt.
	2-0	Rx3 Rate Select (Mode 0)	Rx data rate select, channel 3	
235	7-6	Rx4 AST Control Mode	Rx application select, channel 4	RW
EBh	5-0	Rx4 AST Select Index (Mode 2)		Opt.
	2-0	Rx4 Rate Select (Mode 0)	Rx data rate select, channel 4	
236	7-6	Rx5 AST Control Mode	Rx application select, channel 5	RW
ECh	5-0	Rx5 AST Select Index (Mode 2)		Opt.
	2-0	Rx5 Rate Select (Mode 0)	Rx data rate select, channel 5	
237	7-6	Rx6 AST Control Mode	Rx application select, channel 6	RW
EDh	5-0	Rx6 AST Select Index (Mode 2)		Opt.
	2-0	Rx6 Rate Select (Mode 0)	Rx data rate select, channel 6	
238	7-6	Rx7 AST Control Mode	Rx application select, channel 7	RW
EEh	5-0	Rx7 AST Select Index (Mode 2)		Opt.
	2-0	Rx7 Rate Select (Mode 0)	Rx data rate select, channel 7	
239	7-6	Rx8 AST Control Mode	Rx application select, channel 8	RW
EFh	5-0	Rx8 AST Select Index (Mode 2)		Opt.
	2-0	Rx8 Rate Select (Mode 0)	Rx data rate select, channel 8	
240	7	Rx8 Channel Fault Squelch	Disable all FAWS reports from Rx bit 7	RW
F0h	6	Rx7 Channel Fault Squelch	Disable all FAWS reports from Rx bit 6	Opt.
	5	Rx6 Channel Fault Squelch	Disable all FAWS reports from Rx bit 5	
	4	Rx5 Channel Fault Squelch	Disable all FAWS reports from Rx bit 4	
	3	Rx4 Channel Fault Squelch	Disable all FAWS reports from Rx bit 3	
	2	Rx3 Channel Fault Squelch	Disable all FAWS reports from Rx bit 2	

	1	Rx2 Channel Fault Squelch	Disable all FAWS reports from Rx bit 1	
	0	Rx1 Channel Fault Squelch	Disable all FAWS reports from Rx bit 0	
241 F1h	7	Tx8 Channel Fault Squelch	Disable all FAWS reports from Tx bit 7	RW Opt.
	6	Tx7 Channel Fault Squelch	Disable all FAWS reports from Tx bit 6	
	5	Tx6 Channel Fault Squelch	Disable all FAWS reports from Tx bit 5	
	4	Tx5 Channel Fault Squelch	Disable all FAWS reports from Tx bit 4	
	3	Tx4 Channel Fault Squelch	Disable all FAWS reports from Tx bit 3	
	2	Tx3 Channel Fault Squelch	Disable all FAWS reports from Tx bit 2	
	1	Tx2 Channel Fault Squelch	Disable all FAWS reports from Tx bit 1	
	0	Tx1 Channel Fault Squelch	Disable all FAWS reports from Tx bit 0	
242 F2h	7	Rx8 Power Down	Power down Rx data path, channel 8	RW Opt.
	6	Rx7 Power Down	Power down Rx data path, channel 7	
	5	Rx6 Power Down	Power down Rx data path, channel 6	
	4	Rx5 Power Down	Power down Rx data path, channel 5	
	3	Rx4 Power Down	Power down Rx data path, channel 4	
	2	Rx3 Power Down	Power down Rx data path, channel 3	
	1	Rx2 Power Down	Power down Rx data path, channel 2	
	0	Rx1 Power Down	Power down Rx data path, channel 1	
243 F3h	7	Tx8 Power Down	Power down Tx data path, channel 8	RW Opt.
	6	Tx7 Power Down	Power down Tx data path, channel 7	
	5	Tx6 Power Down	Power down Tx data path, channel 6	
	4	Tx5 Power Down	Power down Tx data path, channel 5	
	3	Tx4 Power Down	Power down Tx data path, channel 4	
	2	Tx3 Power Down	Power down Tx data path, channel 3	
	1	Tx2 Power Down	Power down Tx data path, channel 2	
	0	Tx1 Power Down	Power down Tx data path, channel 1	
244 F4h	7	Rx8 Polarity Flip	Rx data polarity flip, channel 8	RW Opt.
	6	Rx7 Polarity Flip	Rx data polarity flip, channel 7	
	5	Rx6 Polarity Flip	Rx data polarity flip, channel 6	
	4	Rx5 Polarity Flip	Rx data polarity flip, channel 5	
	3	Rx4 Polarity Flip	Rx data polarity flip, channel 4	
	2	Rx3 Polarity Flip	Rx data polarity flip, channel 3	
	1	Rx2 Polarity Flip	Rx data polarity flip, channel 2	
	0	Rx1 Polarity Flip	Rx data polarity flip, channel 1	
245 F5h	7	Tx8 Polarity Flip	Tx data polarity flip, channel 8	RW Opt.
	6	Tx7 Polarity Flip	Tx data polarity flip, channel 7	
	5	Tx6 Polarity Flip	Tx data polarity flip, channel 6	
	4	Tx5 Polarity Flip	Tx data polarity flip, channel 5	
	3	Tx4 Polarity Flip	Tx data polarity flip, channel 4	
	2	Tx3 Polarity Flip	Tx data polarity flip, channel 3	
	1	Tx2 Polarity Flip	Tx data polarity flip, channel 2	
	0	Tx1 Polarity Flip	Tx data polarity flip, channel 1	
246 to 251	All	Reserved		

Note: FAWS = Fault, Alarm, Warning, Status
The setting of any bit in upper page 3 byte 240 inhibits the setting of the corresponding bit in lower page bytes 3 (Rx LOS), 5 (Rx CDR LOL), 10 (Rx Low Power Warning), 11 (Rx Low Power Alarm), 12 (Rx High Power Alarm), 17 (Raw Rx LOS) and 19 (Raw Rx CDR Lock State).

The setting of any bit in upper page 3 byte 241 inhibits the setting of the corresponding bit in lower page bytes 4 (Tx LOS), 6 (Tx CDR LOL), 7 (Tx Fault), 13 (Tx Bias Low Alarm), 14 (Tx Bias High Alarm), 15 (Tx Low Power Alarm), 16 (Tx High Power Alarm), 18 (Raw Tx LOS), 20 (Raw Tx CDR Lock State) and 21 (Raw Tx Fault).

7.4.5.4 Hardware/Firmware ID

The Hardware/Firmware ID fields provide vendor-specific information about the construction of the module. This information is necessary for determining the suitability of doing embedded firmware upgrades in the field. The Hardware/Firmware ID information is as follows:

Table 48- Hardware/Firmware ID (Page 03h, active modules only)

Byte	Bits	Name	Description	Type
252 FCh	All	Reserved		
253 FDh	All	Reserved		
254 FEh	All	F/W major rev	Major revision number of the embedded firmware. This value is the number to the left of the decimal point in the revision number; for example, a value of 2 indicates revision 2.xx	RO Opt.
255 FFh	All	F/W minor rev	Minor revision number of the embedded firmware. This value is the number to the right of the decimal point in the revision number; for example, a value of 27 indicates revision x.27	RO Opt.